NanoMind HP MK3

Datasheet

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Product name: NanoMind HP MK3

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Confidentiality Notice

List of abbreviations

Acronyms	Definitions
AI	Artificial Intelligence
BSP	Board Support Package
CAN	Controller Area Network
CLK	Clock
DDR	Double Data Rate
DS	Datasheet
DUT	Design Under Test
eMMC	embedded MultiMediaCard
FPGA	Field-Programmable Gate Array
FTDI	Future Technology Devices International Limited
GB	GigaByte
GND	Ground
HDL	Hardware Description Language
HLOS	High Level Operating System
HP	High Performance
HW	Hardware
I/O or IO	Input/Output
I2C	Inter-Integrated Circuit
IOPS	Input/output Operations Per Second
IP	Intellectual Property
JTAG	Joint Test Action Group
LDO	Low Dropout
LVCMOS	Low Voltage Complementary Metal Oxide Semiconductor
LVDS	Low-Voltage Differential Signaling
MB	MegaByte
MIO	Multiplexed Input/Output
ML	Machine Learning
MLC	Multi Level Cell
MTU	Maximum Transmission Unit
NC	Not Connected
PCB	Printed Circuit Board
PDK	Platform Development Kit
PL	Programmable Logic
PPS	Pulse Per Second
PS	Processing System
pSLC	pseudo Single Level Cell
PWR	Power
RAM	Random-Access Memory
SCL	Serial Clock
SDA	Serial Data
SDK	Software Development Kit
SE	Single Ended
SIGNIT	Signals Intelligence
SoC	System on Chip
SPW	SpaceWire
SW	Software
TCK	Test Clock
TCP	Transmission Control Protocol
TDI	Test Data In
TDO	Test Data Out
TMS	Test Mode Select
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver Transmitter
UDP	User Datagram Protocol
USB	Universal Serial Bus
YP	Yocto Project

Table of Contents

1 Overview

Figure 1.1: NanoMind HP MK3

1.1 Highlighted Features

- Xilinx Zynq 7030/7045 Programmable SoC
  - Dual ARM Cortex A9 MPCore, up to 800MHz
  - Powerful FPGA with 125k/350k logic cells
- 1GB DDR3 RAM
  - 512MB with Error Correction Code enabled
- 256GB NOR flash
- 70GB eMMC (pSLC) and 233GB eMMC (MLC)
  - HW Bit-Flip Detection
  - Redundant Firmware Image
- High speed interfaces
  - SpaceWire
  - USB (host/device)

1.2 Description

GomSpace NanoMind HP MK3 provides a High Performance, reliable, customizable and flexible onboard computer platform for Payload applications. It has been designed to support High Performance, yet efficient, onboard processing and HW acceleration functions, needed to meet the increasing demands of complex payloads.

The NanoMind HP MK3 is a high performance, versatile Space-graded compute platform based on Xlilinx's Powerful Zynq®-7000 System on a Chip (SoC) family The Zynq®-7030/45 parts integrate a dual-core ARM® Cortex™-A9 based processing system (PS) with a Xilinx FPGA in a single device (programmable logic, PL). This combination allows rapid software prototyping and acceleration of custom programmable hardware development.

NanoMind HP MK3 includes development kits for getting started with software application and FPGA development. The development kits are actively maintained against new Linux BSP- and tool releases from Xilinx, as well as new features introduced by various open-source components within the Yocto Project.
GomSpace also offers a training program to kick-start and support customer development process.

1.3 Applications

Typical customer applications include data reduction using compression algorithms, and Artificial Intelligence (AI) and Machine Learning (ML) for Earth Observation or SIGINT missions. If security and reliability are of concern, then the NanoMind HP MK3 is a perfect HW acceleration platform for Encryption and Error Correction for Command and Data security.

With a wide range of interfaces, configurable I/O and support for in orbit updates, the NanoMind HP MK3 is a highly flexible platform. The included comprehensive development kits are designed to accelerate time to market for custom application development and can also be supplemented with training.

2 Absolute Maximum Ratings

Parameter	Connectors	Min Value	Max Value	Unit
Supply Voltage (Main/Backup) V_{in}	J19, J20	-0.3	36	V
SpaceWire / LVDS voltage levels	J7, J8, J9, J10	-0.4	2.6	V
CAN voltage levels	J5, J6, J15, J16, J17	-60	60	V
RS422/RS485 voltage levels	J5, J6, J11, J13, J14	0	4	V
CLK voltage levels	J5, J6	-0.3	2.0	V
I2C voltage levels	J5, J6	-0.3	7.0	V
PPS voltage levels	J5, J6	-0.5	4.0	V
IO voltage levels	J4, J12, J18	-0.3	3.6	V
USB voltage levels	J2	-0.3	6	V
Thermal interface temperature		-40	50	°C
Storage Temperature		-40	85	°C

Table 2.1: Absolute maximum ratings

*Ratings given in this table are the absolute maximum values the device can handle under stress or transient conditions. The device should **not** be operated under these conditions. Exceeding these values may cause permanent damage to the NanoMind HP MK3 assembly and/or externally connected devices. Please refer to section 8 for recommended operating conditions.*

3 Block Diagram

A high-level block diagram of the product is provided in Figure 3.1. Note that the daughter board slots are shielded for the NanoMind HP MK3 product and are available only for a set of derived products.

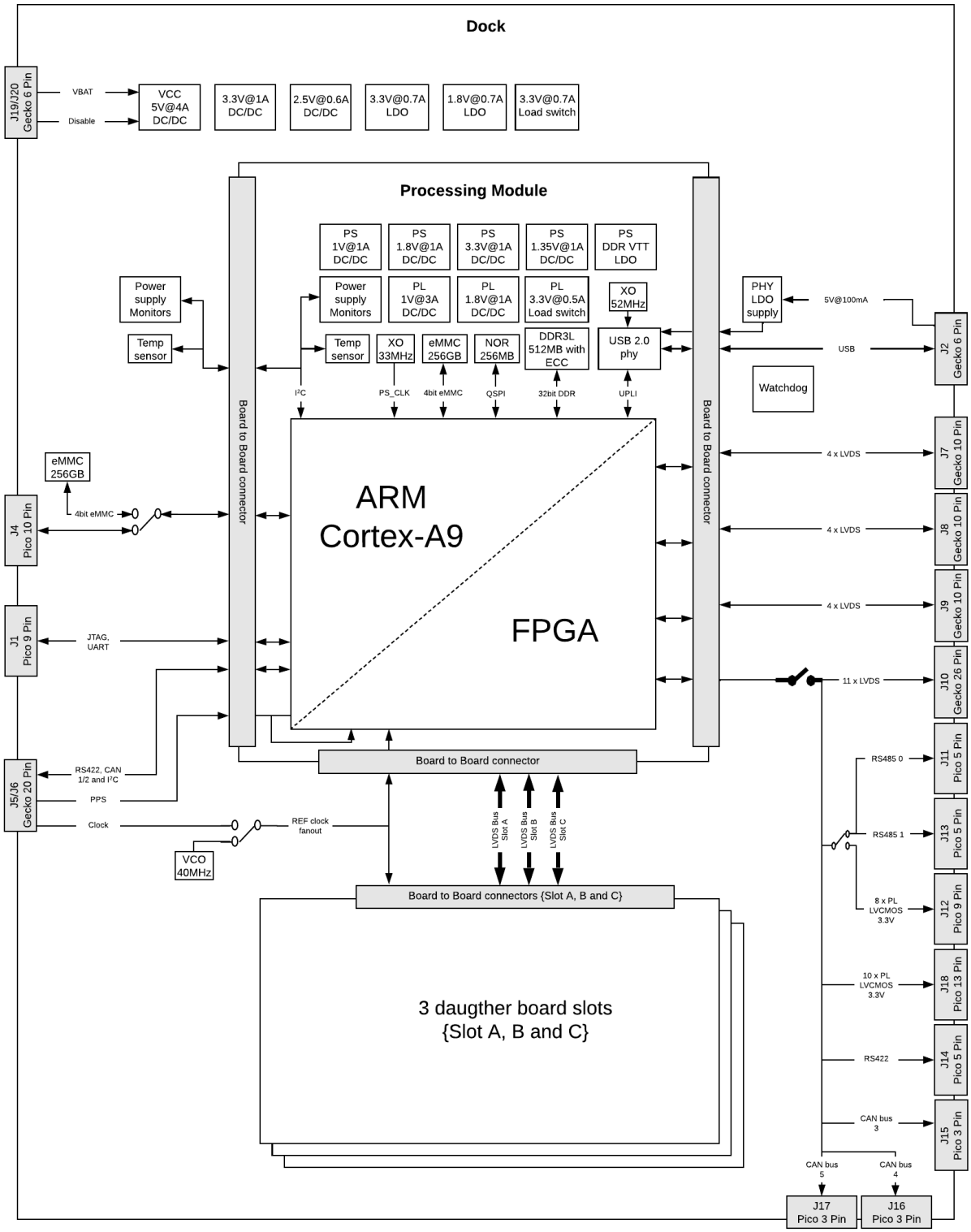

Figure 3.1: NanoMind HP MK3 Block diagram

4 Thermal Characteristics

The thermal interface of the unit is defined on the mechanical connection point marked with red square in Figure 4.1.
The NanoMind HP MK3 has been qualified to an operational temperature range from -40°C to 50°C and a non-operational temperature range from -40°C to 85°C.

The most critical circuit has a maximum operational temperature of 85°C. At an interface temperature of 53°C, the most critical circuit temperature is 82°C at maximum operational power, so a maximum interface temperature 50°C gives sufficient margin to ensure that the most critical circuit is below 85°C.

Higher interface temperatures can be tolerated if it is ensured that the different modules all remain below 85°C.

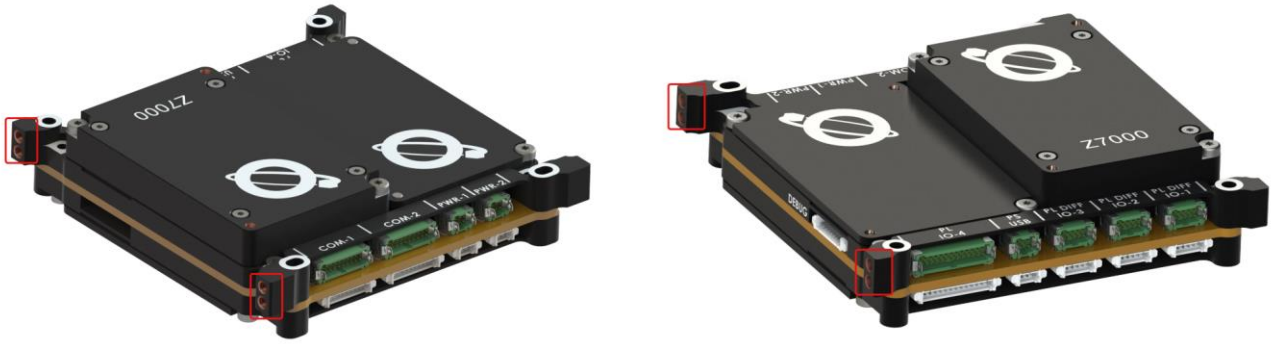

Figure 4.1: Thermal interface

5 Mechanical Characteristics

Description	Value	Unit
Mass total (typical)	240	g
Size (L x W x H)	95 x 95 x 24,15	mm

Table 5.1: Mechanical properties

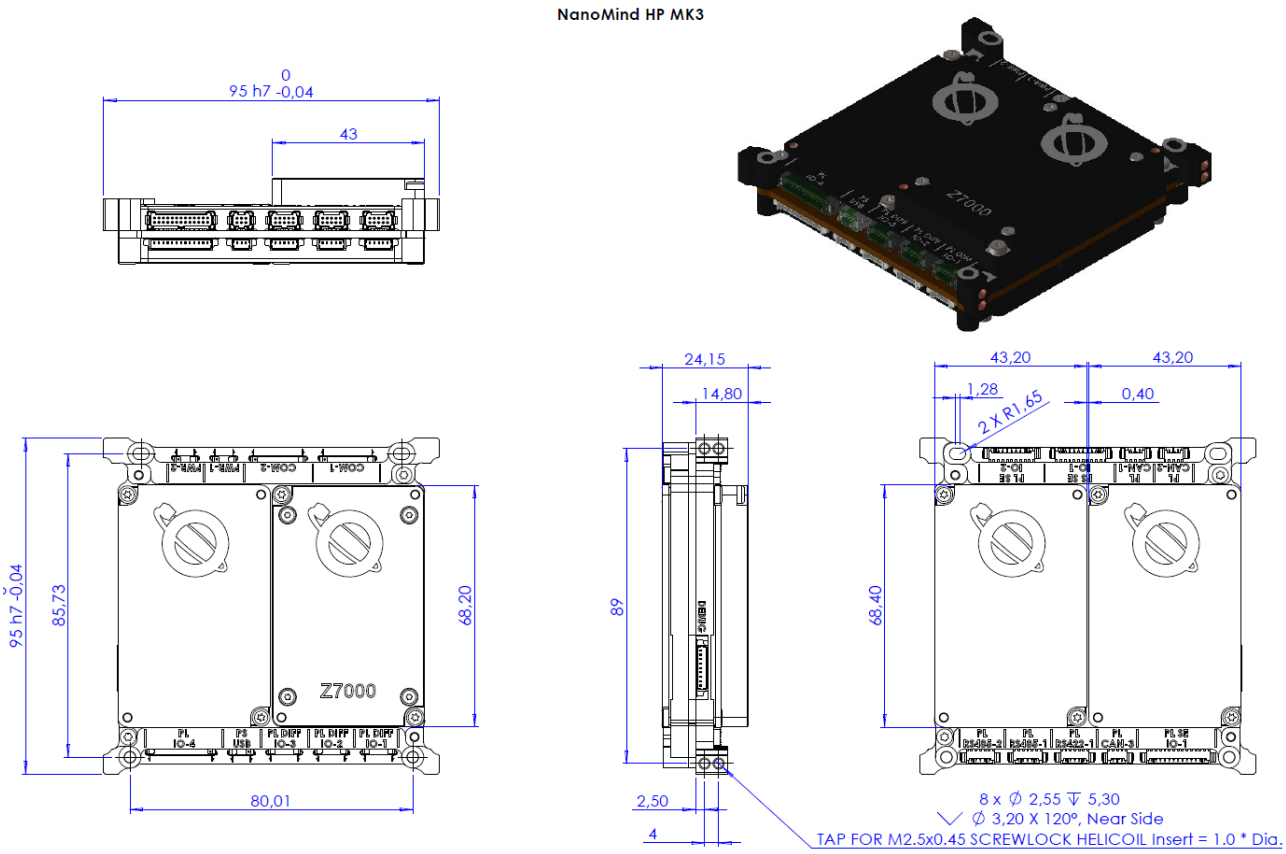

Figure 5.1: NanoMind HP MK3 mechanical drawing (all dimensions are in mm)

6 Connectors overview

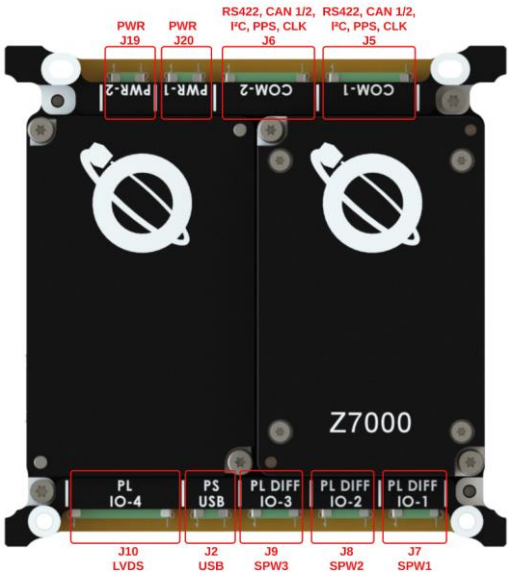

Figure 6.1: NanoMind HP MK3 top view

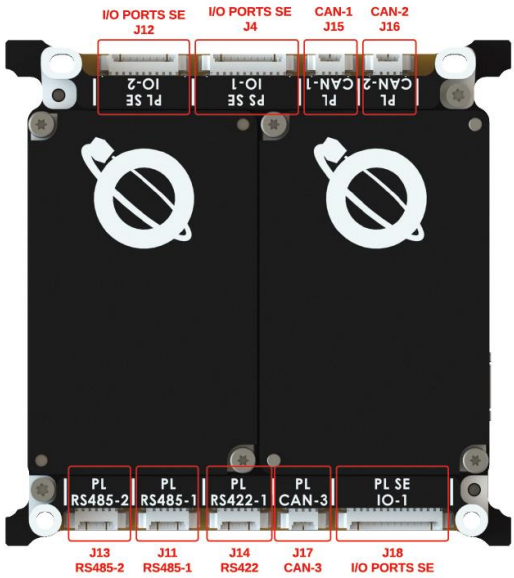

Figure 6.2: NanoMind HP MK3 bottom view

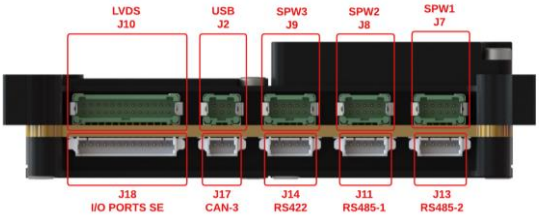

Figure 6.3: NanoMind HP MK3 front view

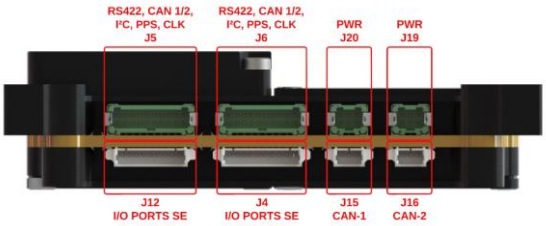

Figure 6.4: NanoMind HP MK3 back view

Figure 6.5: NanoMind HP MK3 left side view

7 Included Cable kit

Cables necessary for interfacing with the NanoMind HP MK3 product for initial bring-up are included with the product. This includes power cables and main interfaces. Below is an overview of cables included with the product for debug/ test purpose only:

Name	Connection	GomSpace ID	Length	Description
PWR	PWR-1 (J20) or PWR-2 (J19)	110448	50cm	Power harness to flying leads
DB1	DEBUG (J1)	108562	3.5cm	Debug harness
DB2	DB1	108558	N.A.	Debug breakout PCB
DB3	DB2	103011	N.A.	FTDI USB-TTL serial cable
DB4	DB2	104557	1200 cm	JTAG-HS3 & USB A to MICRO USB B
USB	USB (J2)	108560	1000 cm	USB Cable
Main Bus	COM-1 (J5) or COM-2 (J6)	108559	15 cm	Main Bus Harness Flying Leads

Table 7.1: Product cable kit content

The location of the required individual connectors is documented in separate section with detailed connector pinout for all interfaces.

8 Electrical Characteristics

8.1 Power Characteristics

The current value in the Table 8.1 below was measured with a Zynq 7045 at 25°C.

Parameter	Condition	Min	Typ	Max	Unit
Supply Current (Main/Backup)	V_{in} = 12V, Idle[1], 25°C		150		mA
	V_{in} = 18V, Idle[1], 25°C		103		mA
	V_{in} = 24V, Idle[1], 25°C		80		mA
	V_{in} = 32V, Idle[1], 25°C		65		mA

Table 8.1: Current consumption values

[1] Linux running in idle, default after startup, no PL services running, no external devices.

8.2 Interfaces Characteristics

Interface	Connector	Parameter	Min	Typ	Max	Unit
V_{in}	J19, J20	Supply voltage (Main/Backup)	12		32	V
SpaceWire/LVDS	J7, J8, J9, J10	Differential input voltage	100	350	600	mV
		Common mode input voltage	0.30	1.20	1.5	V
		Differential output voltage	247	350	600	mV
		Common mode output voltage	1.00	1.25	1.425	V
CAN	J5, J6, J15[1], J16[1], J17[1]	Differential input threshold voltage	0.50		0.90	V
		Common mode input voltage			±25	V
		Differential output threshold voltage (recessive)	-500	0	50	mV
		Differential output threshold voltage (dominant)	1.5	2.2	3.0	V
		Common mode output voltage (dominant)	1.45	1.95	2.45	V
RS422[2]/ RS485[2]	J5, J6, J11, J13, J14	Differential Input Threshold	-0.20		0.20	V
		Receiver input voltage range	0		4	V
		Differential output voltage	2.0			V
		Common mode output voltage			3	V
CLK	J5, J6	Differential input voltage		150		mV
		Common mode input voltage	1.55		1.7	V
I2C	J5, J6	Input logic high voltage		3.3		V
		SDA, SCL Logic input threshold voltage	1.6	1.8	2	V
		Input logic low voltage			0.4	V
		Output logic high voltage		3.30		V
		Output logic low voltage	0	0.19	0.3	V
PPS	J5, J6	Logic power supply voltage		3.3		V
		Differential Input Voltage	0.10		0.60	V
		Common mode input range	0.05		2.45	V
IO	J4, J12, J18	High-level input voltage	2.15	3.30	3.30	V
		Low-level input voltage	0	0	0.8	V
	J4	High-level output voltage, @ -16mA	2.90	3.30		V
		Low-level output voltage @ 16mA		0	0.4	V
		Maximum output current[3]	-16		16	mA
	J12[4], J18[4]	High-level output voltage, @ -20uA	2.90	3.30		V
		Low-level output voltage @ 20uA		0	0.4	V
		Maximum output current	-20		+20	uA

Table 8.2: Input and output characteristics

[1] Need PL license for implementation, see section 9.10 for more details.

[2] The RS422 and RS485 input with 120Ω differential termination between RS4xx-RX-P and RS4xx-RX-N terminals. For failsafe operation the differential input is equipped with a resistive divider network to terminate the input of the RS4xx transceiver when nothing is connected. The resistive network consists of a 390Ω pullup via a Schottky diode to 3.3V supply and a 390Ω pulldown to GND (see Figure 8.1 below).

[3] SoC configurable to supported drive strengths of 4, 8, 12, or 16 mA.

[4] It can only translate push-pull CMOS logic outputs.

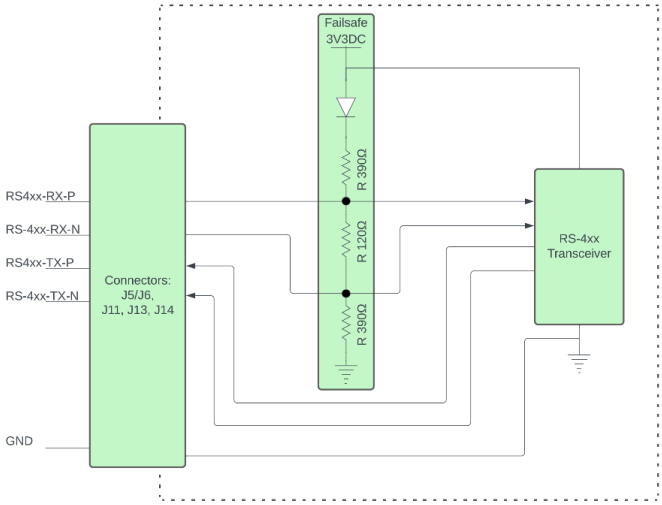

Figure 8.1: RS422 and RS485 interface

9 Connectors and Pin Functions

9.1 PWR-1 and PWR-2 (J19-J20)

NanoMind HP MK3 is equipped with two Harwin Gecko G125-MH10605L1R 1.25mm pitch high-reliability connectors, with latches, for external power supply. The board can be supplied through either connector, PWR-1 or PWR-2, using a single power supply or by connecting two independent power supplies for redundancy. A supply balancing circuit automatically selects whichever of the two power connectors that carries the highest VIN voltage as supply source. The load will be shared between the two power connectors if the extern supply voltages VIN1 and VIN2 are of equal levels.

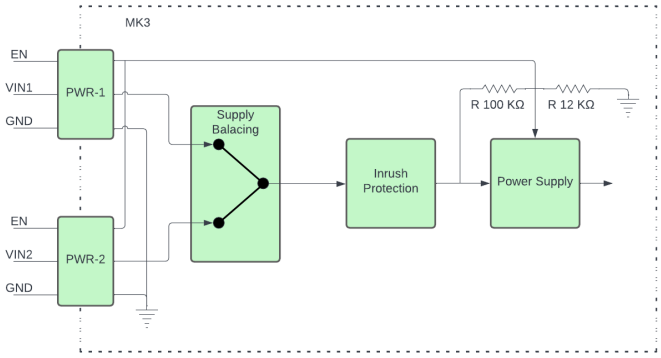

Figure 9.1: NanoMind HP MK3 power supply interface

An external supply EN control pin makes it possible to enable or disable the DC/DC converter supplying the NanoMind HP MK3 independent of the supply voltage. The feature can be omitted by leaving the external EN control pin not connected. The EN pins from PWR-1 and PWR-2 are internally connected.

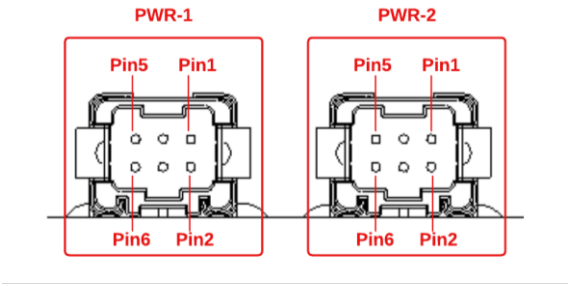

Figure 9.2: PWR-1 and PWR-2 pinout

Pin	PWR-1 Signal	PWR-2 Signal	Description
1	VIN1	VIN2	Supply voltage VCC (12V to 32V)
2	EN	EN	Supply enable signal, internally tied to Vin through a 100kΩ / 12kΩ divider. EN Low = 0V to 0.8V: Power supply / NanoMind HP MK3 is OFF EN High = 1.2V to 24V: Power supply / NanoMind HP MK3 is ON If enable function is not used, this pin shall be left unconnected and the NanoMind HP MK3 will automatically turn on/off with the supply voltage.
3	VIN1	VIN2	Supply voltage VCC (12V to 32V)
4	GND	GND	Ground
5	VIN1	VIN2	Supply voltage VCC (12V to 32V)
6	GND	GND	Ground

Table 9.1: PWR-1 and PWR-2 pin allocation

9.2 CAN and RS422 - COMM 1-2 (J5-J6)

NanoMind HP MK3 is equipped with two Harwin Gecko G125-MH12005L1R 1.25mm pitch high-reliability connectors, with latches, for access to its main communication interface. The individual pins of the two connectors are interconnected, which allow the Nanomind to use with in different bus topologies. The secondary connector can be used for interconnecting with other devices in multidrop bus configuration or for bus terminations if it is the last node in the system.

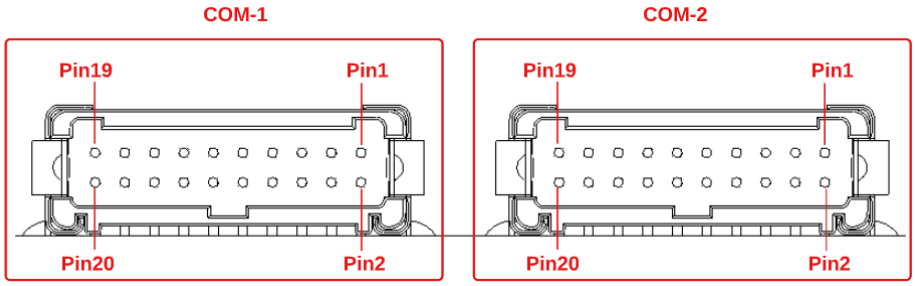

Figure 9.3: COM-1 and COM-2 pinout

Pin	Signal	Description
1	I2C-SDA	I2C serial data line[1]
2	CAN1_H	CAN1 High[2]
3	GND	Ground
4	CAN1_L	CAN1 Low[2]
5	I2C-SCL	I2C serial clock line[1]
6	CAN2_H	CAN2 High[2]
7	GND	Ground
8	CAN2_L	CAN2 Low[2]
9	PPS-P	Pulse Per Second LVDS positive input line[3]
10	CLK-P	External reference clock LVDS positive input line
11	PPS-N	Pulse Per Second LVDS negative input line[3]
12	CLK-N	External reference clock LVDS negative input line
13	NC	Not connected
14	RS422-TX-P	RS422 Noninverting driver output for payload data interface
15	GND	Ground
16	RS422-TX-N	RS422 Inverting driver output for payload data interface
17	NC	Not connected
18	RS422-RX-P	RS422 Noninverting receiver input for payload data interface[4]
19	GND	Ground
20	RS422-RX-N	RS422 Inverting receiver input for payload data interface[4]

Table 9.2: COM-1 and COM-2 pin allocation

[1] Discrete 2.4kΩ pull-up resistor to 3.3V. Multi-master/CSP not supported by SW drivers, only connect slave devices.

[2] CAN1 and CAN2 are without any differential termination between CAN_H and CAN_L

[3] No discrete termination, 100Ω resistor shall be added between PPS-P and PPS-N if used.

[4] Discrete 120Ω termination between RS422-RX-P and RS422-RX-N and discrete pull-up/pull-down termination for failsafe operation, see Figure 8.1.

9.3 SpaceWire – PL DIFF 1-3 (J7-J8-J9)

NanoMind HP MK3 is equipped with three independent bi-directional, full-duplex SpaceWire interfaces for payload data transfer. It uses Gecko G125-MH11005L1R 1.25mm pitch high-reliability connectors, with latches from Harwin for each of the three interfaces:

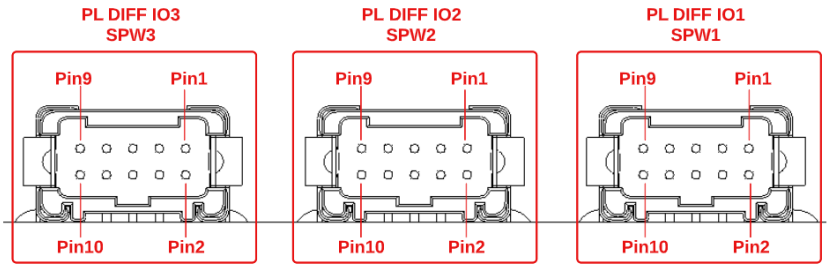

Figure 9.4: SPW1, SPW2 and SPW3 pinout

Each SpaceWire[1] interface uses two signals, data and strobe, in receive and transmit direction to send serial bit streams. The signals are based on low voltage differential signals according to the ANSI TIA/EIA-644 Standard and requires two pins for each signal. The signals are named:

Pin	Signal	Description
1	Dout-	LVDS Data output negative line
2	Sin+	LVDS Strobe input positive line[2]
3	Dout+	LVDS Data output positive line
4	Sin-	LVDS Strobe input negative line[2]
5	GND	Ground connection for internal cable shielding[3]
6	GND	Ground connector for external cable shielding[3]
7	Sout-	LVDS Strobe output negative line
8	Din+	LVDS Data input positive line[2]
9	Sout+	LVDS Strobe output positive line
10	Din-	LVDS Data input negative line[2]

Table 9.3: SPW-1, SPW-2 and SPW-3 pin allocation

[1] Can be repurposed for other protocols through development kit.

[2] Differential 100Ω termination resistor configurable in the SoC.

[3] Two pins for internal and external cable shielding are provided as well in each SpaceWire interface. A SpaceWire cable contains four twisted pair of wires with a characteristic impedance of 100Ω. In case of shielding, it is possible to uses those pins to terminate internally (around each twisted pair) and externally shielding by connecting to those pins.

9.4 PL Differential Input/Output – PL IO-4 (J10)

NanoMind HP MK3 is equipped with 11 Low Volage Differential Signaling (LVDS) pairs used for general purpose. It uses a Gecko G125-MH12605L1P 1.25mm pitch high-reliability connector, with latches from Harwin:

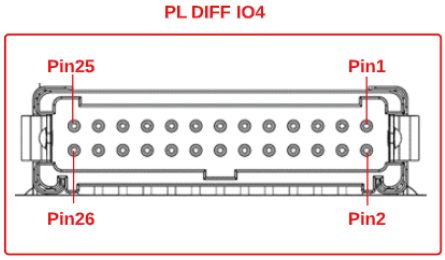

Figure 9.5: PL DIFF IO-4 LVDS pinout

These pins are unused in the GomSpace provided reference design but can be configured with the development kit. Differential 100Ω input termination resistor can be configured in the SoC.

Pin	Signal	Description
1	LVDS1-P	LVDS1 positive line
2	GND	Ground
3	LVDS1-N	LVDS1 negative line
4	LVDS2-P	LVDS2 positive line
5	LVDS3-P	LVDS3 positive line
6	LVDS2-N	LVDS2 negative line
7	LVDS3-N	LVDS3 negative line
8	GND	Ground
9	LVDS4-N	LVDS4 negative line
10	LVDS5-P	LVDS5 positive line
11	LVDS4-P	LVDS4 positive line
12	LVDS5-N	LVDS5 negative line
13	LVDS6-P	LVDS6 positive line
14	LVDS7-P	LVDS7 positive line
15	LVDS6-N	LVDS6 negative line
16	LVDS7-N	LVDS7 negative line
17	GND	Ground
18	LVDS8-P	LVDS8 positive line
19	LVDS9-P	LVDS9 positive line
20	LVDS8-N	LVDS8 negative line
21	LVDS9-N	LVDS9 negative line
22	LVDS10-P	LVDS10 positive line
23	LVDS11-P	LVDS11 positive line
24	LVDS10-N	LVDS10 negative line
25	LVDS11-N	LVDS11 negative line
26	GND	Ground

Table 9.4 : PL DIFF IO-4 LVDS pin allocation

9.5 PL Single Ended Input/Output 1– PL SE IO-1 (J18)

NanoMind HP MK3 is equipped with 10 single-ended (SE) input/output used for general purpose. It uses a Picoblade 532611371 1.25mm pitch high-reliability connector from Molex:

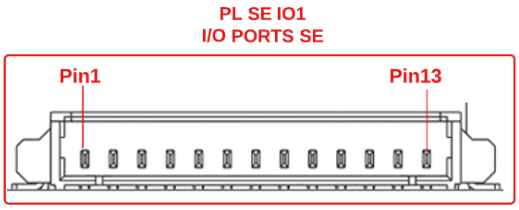

Figure 9.6: PL SE IO-1 pinout

These pins are unused in the GomSpace provided reference design but can be configured with the development kit.

Pin	Signal	Description
1	GND	Ground
2	IO1	SE Input/Output 1
3	IO2	SE Input/Output 2
4	IO3	SE Input/Output 3
5	IO4	SE Input/Output 4
6	IO5	SE Input/Output 5
7	GND	Ground
8	IO6	SE Input/Output 6
9	IO7	SE Input/Output 7
10	IO8	SE Input/Output 8
11	IO9	SE Input/Output 9
12	IO10	SE Input/Output 10
13	GND	Ground

Table 9.5: PL SE IO-1 pin allocation

9.6 PL Single Ended Input/Output 2– PL SE IO-2 (J12)

NanoMind HP MK3 can be equipped with additional 8 single-ended (SE) input/output used for general purpose if RS485 is not used (on J11-J13). It uses a Picoblade 532610971 1.25mm pitch high-reliability connector from Molex:

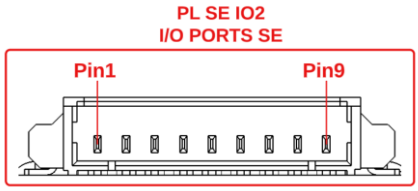

Figure 9.7: PL SE IO-2 pinout

These pins (Table 9.6 in next pages) are unused in the GomSpace provided reference design but can be configured with the development kit. PL SE IO-2 (J12) and RS485 (J11-J13) connectors are mutually exclusive. By default, RS485 is configured for use in the SoC.

Pin	Signal	Description
1	IO1	SE Input/Output 1
2	IO2	SE Input/Output 2
3	IO3	SE Input/Output 3
4	IO4	SE Input/Output 4
5	GND	Ground
6	IO5	SE Input/Output 5
7	IO6	SE Input/Output 6
8	IO7	SE Input/Output 7
9	IO8	SE Input/Output 8

Table 9.6: PL SE IO-2 pin allocation

9.7 PS Single Ended Interface – PS SE IO-1 (J4)

NanoMind HP MK3 is equipped with 6 single-ended Multiplexed Input/Output (MIO) used for general purpose. It uses a Picoblade 532611071 1.25mm pitch high-reliability connector from Molex:

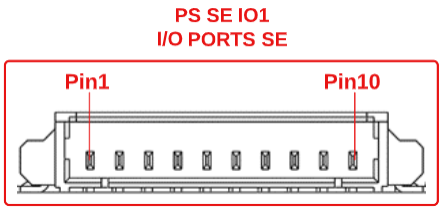

Figure 9.8: PS SE IO-1 pinout

These pins are unused in the GomSpace provided reference design but can be configured with the development kit. The MIO is shared with the secondary eMMC and cannot be used while this is active.

Pin	Signal	Description
1	IO1	Multiplexed Input/Output 1
2	GND	Ground
3	IO2	Multiplexed Input/Output 2
4	GND	Ground
5	IO3	Multiplexed Input/Output 3
6	GND	Ground
7	IO4	Multiplexed Input/Output 4
8	GND	Ground
9	IO5	Multiplexed Input/Output 5
10	IO6	Multiplexed Input/Output 6

Table 9.7: PS SE IO-1 pin allocation

9.8 RS485 interfaces – PL RS485 1-2 (J11-J13)

NanoMind HP MK3 is equipped with two full duplex RS485 interfaces. It uses a Picoblade 532610571 1.25mm pitch high-reliability connector from Molex:

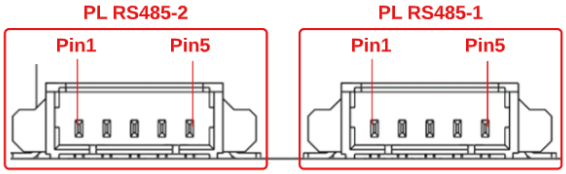

Figure 9.9: RS485 pinout

PL SE IO-2 (J12) and RS485 (J11-J13) connectors are mutually exclusive. By default, RS485 is configured for use in the SoC.

Pin	Signal	Description
1	RS485-TX-N	RS485 Drive Negative
2	RS485-TX-P	RS485 Drive Positive
3	GND	Ground
4	RS485-RX-N	RS485 Receive Negative[1]
5	RS485-RX-P	RS485 Receive Positive[1]

Table 9.8: RS485 pin allocation

[1] Discrete 120Ω termination between RS485-RX-P and RS485-RX-N and discrete pull-up/pull-down termination for failsafe operation, see Figure 8.1.

9.9 RS422 interface – PL RS422-1 (J14)

NanoMind HP MK3 is equipped with a full duplex RS422 interface. It uses a Picoblade 532610571 1.25mm pitch high-reliability connector from Molex:

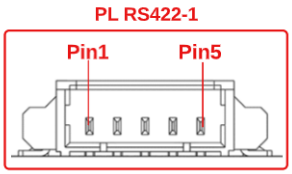

Figure 9.10: RS422 pinout

These pins can only be used for RS422 interface.

Pin	Signal	Description
1	RS422-TX-N	RS422 Drive Negative
2	RS422-TX-P	RS422 Drive Positive
3	GND	Ground
4	RS422-RX-N	RS422 Receive Negative[1]
5	RS422-RX-P	RS422 Receive Positive[1]

Table 9.9: RS422 pin allocation

[1] Discrete 120Ω termination between RS422-RX-P and RS422-RX-N and discrete pull-up/pull-down termination for failsafe operation, see Figure 8.1.

9.10 PL CAN 1-3 * (J15-J16-J17)

NanoMind HP MK3 is equipped with three hardware CAN interfaces. It uses a Picoblade 532610371 1.25mm pitch high-reliability connector from Molex:

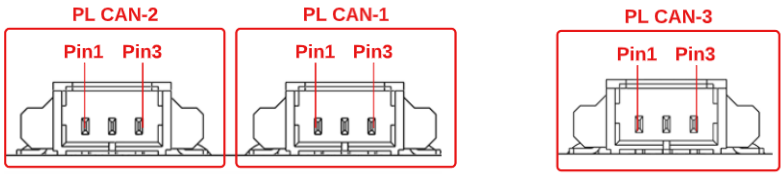

Figure 9.11. CAN pinout

These interfaces are reserved for future use. The IP cores realizing the protocol are not delivered by GomSpace but may be added through the provided development kit. It furthermore requires a proper license agreement with Robert Bosch.

Pin	Signal	Description
1	CAN_H	CAN High[1]
2	CAN_L	CAN Low[1]
3	GND	Ground

Table 9.10: CAN pin allocation

[1] CAN-1 has 120R differential termination between CAN_H and CAN_L. CAN-2 and CAN-3 are without any differential termination between CAN_H and CAN_L.

9.11 Debug and Programming Interface – DEBUG (J1)

NanoMind HP MK3 is equipped with a debug connector including JTAG, UART and Reset. It uses a Picoblade 532610971 1.25mm pitch high-reliability connector from Molex:

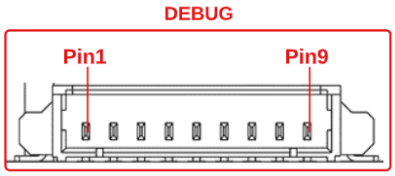

Figure 9.12: Debug and programming pinout

The debug and programming interface is used for development and debugging. The interface is not intended to be used in flight or integrated with the satellite bus.

Pin	Signal	Description
1	TDO	JTAG Test Data Out
2	TCK	JTAG Test Clock
3	TMS	JTAG Test Mode Select
4	TDI	JTAG Test Data In
5	SYS_RST	System Reset
6	3.3V	3.3V from the Nanomind[1]
7	UART_RX	Debug UART DUT Receive Line
8	UART_TX	Debug UART DUT Transmit Line
9	GND	Ground

Table 9.11: DEBUG pin allocation

[1] Maximum output continuous current is +/- 25mA.

9.12 PS USB (J2)

NanoMind HP MK3 is equipped with a Harwin Gecko G125-MH10605L1R 1.25mm pitch high-reliability connectors, with latches, for USB interface.

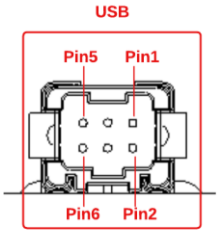

Figure 9.13: USB pinout

The NanoMind HP supports USB 2.0 device and host[1] application on the dedicated USB connector.

Pin	Signal	Description
1	VBUS_IN	USB VBUS 5V input
2	USB D-	USB Data negative
3	VBUS_OUT[1]	USB VBUS 4.6V output – Only for host application. Left unconnected for device application.
4	USB D+	USB Data positive
5	GND	Ground
6	GND	Ground

Table 9.12: USB pin allocation

[1] For host application, connect VBUS_OUT to VBUS_IN. The maximum host VBUS voltage is 4.6V.

10 Performance Characteristics

10.1 eMMC

The eMMC performance characteristics are derived using the "fio" https:/fio.readthedocs.io/en/latest/fio_doc.html benchmarking application. Below tables summarize varying workloads for read, write and simultaneous read/write operations.

Sequential Read	Sequential Write	Sequential Read/write
23 MByte/sec (22 IOPS)	21 MByte/sec (20 IOPS)	11/11 MByte/sec (10/10 IOPS)

Random Read	Random Write	Random Read/write
22 MByte/sec (21 IOPS)	21 MByte/sec (20 IOPS)	11/11 MByte/sec (10/10 IOPS)

Table 10.1: eMMC performances

10.2 SpaceWire

The SpaceWire performance characteristics are derived using the "iperf3" (https://iperf.fr/iperf-doc.php) benchmarking application. The benchmark is thus conducted at the network layer with an MTU of 9000 bytes. Below table summarize the performance for both a single interface and three interfaces transferring data simultaneously for both TCP- and UDP connections.

	TCP	UDP
Single interface	155 Mbit/sec	175 Mbit/sec
Three interfaces	130 Mbit/sec	170 Mbit/sec

Table 10.2: SpaceWire characteristics

10.3 RS-422

The RS-422 performance characteristics are derived using the "iperf3" (https://iperf.fr/iperf-doc.php) benchmarking application. The test is thus conducted at the network layer and below table summarize the performance for each of the two interfaces for TCP transfers.

PS	PL
3 Mbit/sec	2.2 Mbit/sec

Table 10.3: RS-422 characteristics

11 Development Kits Overview

Depending on the level of customization required, two options for development kits are provided. For use cases requiring low level customization (including PL development), a platform development kit (PDK) is provided. On the other hand, for use cases focused on high level software (SW) development, a software development kit (SDK) is provided.
Common for both is that all GomSpace added functionality is provided as source code and thus customizable for specific mission- and usage requirements.

11.1 PDK

GomSpace provides meta information for a complete open-source stack, with U-Boot being the bootloader and Linux the high level operating system (HLOS). The PDK is split in two parts; PL development is facilitated through Xilinx Vivado Design Suite whereas Yocto Project (YP) is the tool used for customizing U-Boot, Linux board support package (BSP), Linux distribution, and associated applications. The relation between these and overall flow is depicted in the Figure 11.1.

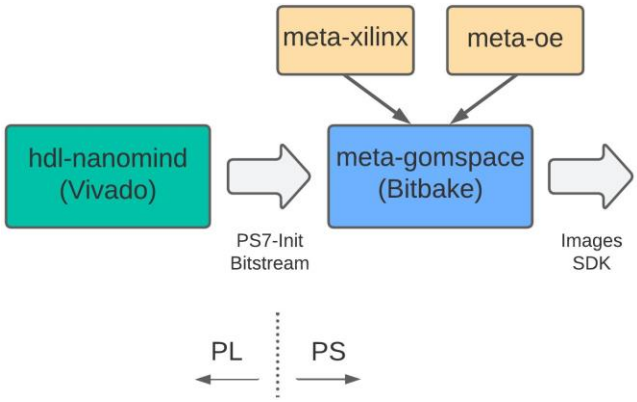

Figure 11.1: Platform Development Kit (PDK)

The intended audience of the PDK are the “advanced” users, that to some degree master both hardware description language (HDL) development as well as low- and high-level SW development. The learning curve of this is generally considered steep, and if this level of customization is not required, it may be worth considering the SDK instead.

11.2 SDK

The SDK is rendered from the PDK by means of a Yocto Project rendered *eSDK*. As the name implies, it targets SW development and is thus described by the right-hand side of the above illustration. The PS part of the PDK is based on a “full” YP environment centered around the *bitbake* tool, whereas the SDK is centered around *devtool* which can be considered a subset of the former. They share the same fundamentals by parsing “recipes” describing how the SW components are built.
The whole PS SW stack is provided as source code, however bitstream is provided synthesized.

12 Qualifications

To simulate the harsh conditions of launch and space, the NanoMind HP MK3 has been exposed to several environmental tests. Contact GomSpace for further information.

13 Disclaimer

The information in this document is subject to change without notice and should not be construed as a commitment by GomSpace. GomSpace assumes no responsibility for any errors that may appear in this document.

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