NanoCom SDR
SDR Dock, Z7000 and TR-600

Datasheet
Software Defined Radio

GomSpace A/S | Langagervej 6 | DK-9220 Aalborg East | Denmark
gomspace.com | sales@gomspace.com | T: +45 71 741 741

Product name: NanoCom SDR

Document No.: 1015263

Revision: 1.0

Author: JESM

Approved by: MJ/TAN

Approval date: 14 November 2018

Confidentiality Notice

Table of Contents

1 Overview

The NanoCom SDR consists of the following products:

- NanoDock SDR
- NanoMind Z7000
- NanoCom TR-600

It is possible, to connect up to three TR-600 to the NanoDock SDR motherboard. Fig. 1-1 shows a NanoCom SDR with a Z7000 and one TR-600.

Fig. 1-1 NanoCom SDR (NanoDock SDR, NanoMind Z7000 and NanoCom TR-600)

The three components are designed to be a modular CPU/FPGA and radio for small satellites. It is built around GomSpace's modular technology, allowing numerous configurations of modules to be implemented on a motherboard, saving significant volume and giving customers a high level of customization.

Further technical specifications of the three individual components can be found in their respective datasheets:

NanoDock SDR:	gs-ds-nanodock-sdr-<version>.pdf
NanoMind Z7000:	gs-ds-nanomind-z7000-<version>.pdf
NanoCom TR-600:	gs-ds-nanocom-tr600-<version>.pdf

The NanoCom SDR supports a modem for each mounted TR-600. In general, the use of one modem will result in better performance.

1.1 Highlighted Features

- GomSpace Mother/Daughter board concept
- Supports the NanoMind Z7000 and 3 NanoCom TR-600s
- Flight proven
- Centralized 40 MHz clock
- Fits standard PC104
- MicroSD card connector
- USB to UART console interface for easy use in lab setup (GOSH)
- Collective mass (NanoDock, Z7000, 1 TR-600 and 2 slot shields): ~ 271 g
- Operational temperature: -40°C to +85°C
- Storage temperature: -40°C to +85°C
- IPC-A-610 Class 3A assembly

NanoDock SDR motherboard

- PCB material: Glass/Polyimide IPC 6012C cl. 3/A

NanoMind Z7000

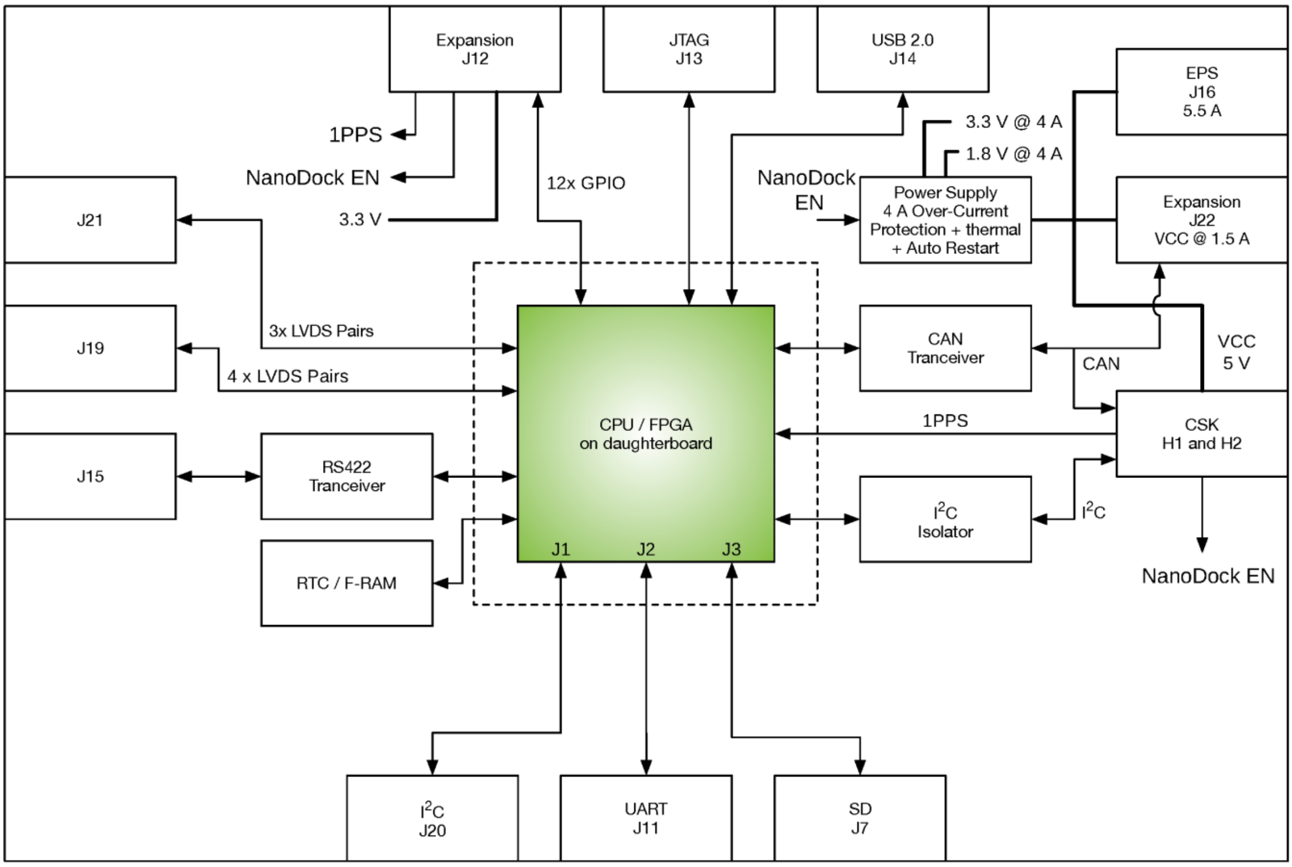
- Xilinx Zync 7030 Programmable SoC
- ARMv7 Architecture
- Dual ARM Cortex A9 MPCore up to 800 MHz (standard clocked at 666 MHz)
- 1 GB DDR3 RAM and 32GB storage (GB: Giga Byte)
- Powerful FPGA module – 125K logic cells
- Precision milled anodized aluminium heat sink to control thermal load and provide EMI shielding
- Linux distribution/operating system
- PCB material: 22-layer glass/polyimide

NanoCom TR-600

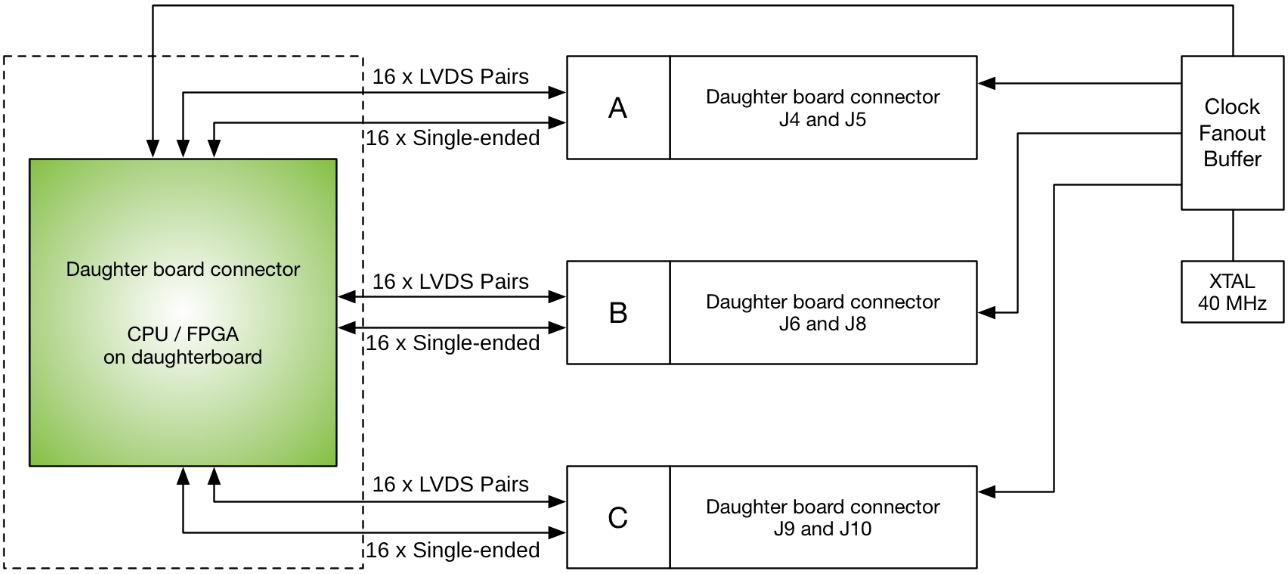
- AD9361 IC
- 2 × 2 transceiver with integrated DACs and ADCs
- Band: 70 MHz to 6 GHz
- Channel bandwidth is tuneable from 200 kHz to 56 MHz
- Supports TDD and FDD operation.
- Multichip synchronization
- LVDS/single-ended digital BB interface
- Flight proven
- Precision milled anodized aluminium heat sink to control thermal load and provide EMI shielding
- Temperature and current sensors
- EEprom for persistent configuration storage
- PCB material: glass/polyimide ESA ECSS-Q-ST-70-11-C

1.2 Block Diagram

1.2.1 CPU/FPGA and Connectors



1.2.2 CPU/FPGA Connection to Daughterboards



2 Connector Pinout

The pinouts of the NanoCom SDR are described in the following sub-sections.

2.1 NanoDock SDR Top

The connectors of the NanoDock SDR are shown in Fig. 2-1. The TR-600 is placed in Slot A.

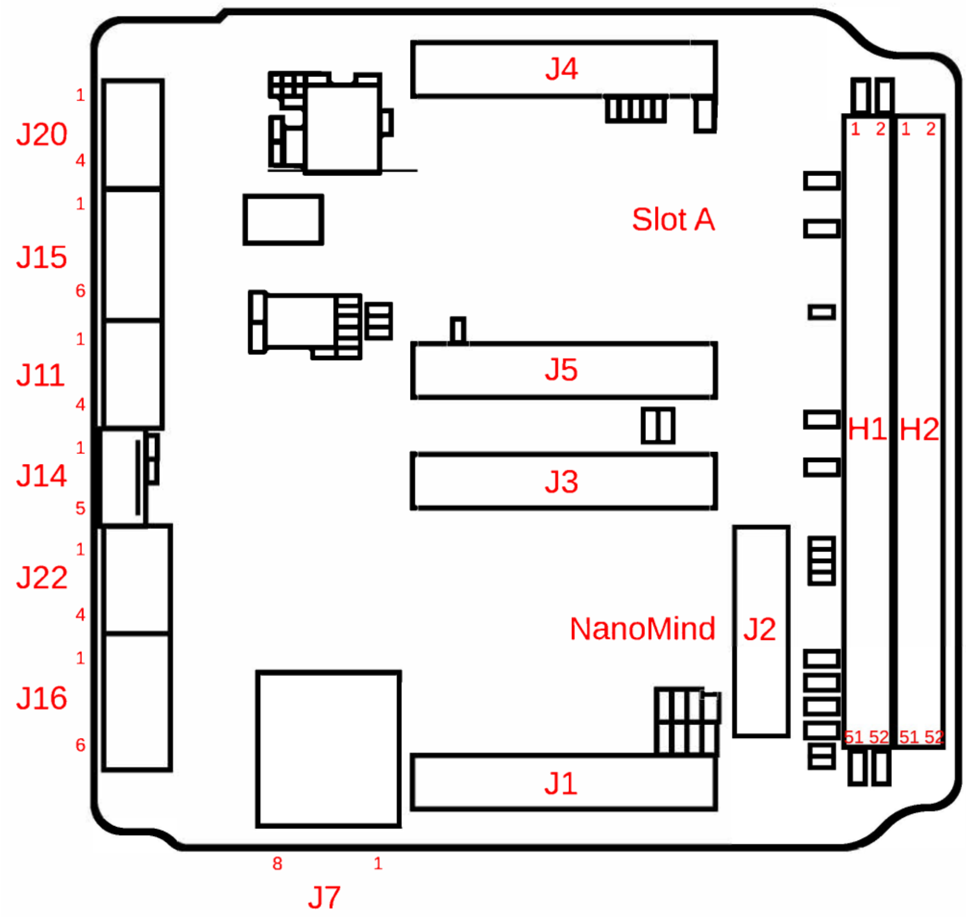


Fig. 2-1 NanoDock SDR (top)

2.1.1 H1/H2 – Stack Connector

The relevant pins are listed in the tables below.

H1

Pin	Description
1	CANL *
2	GPS heartbeat *
3	CANH *
41	CSK_SDA *
43	CSK_SCL *
45	GND *
46	GND *
47	VCC input option *
48	VCC input option *
49	VCC input option *
50	VCC input option *
51	VCC input option *
52	VCC input option *

H2

Pin	Description
1	VCC input option *
2	VCC input option *
3	VCC input option *
4	VCC input option *
5	VCC input option *
6	VCC input option *
7	GND *
8	GND *
27	VCC input option *
28	VCC input option *
29	GND
30	GND
32	GND
49	VCC input option *
51	VCC input option *

* Depending on option sheet choice

It is recommended to use connector J16 to power the NanoDock SDR. Powering through the stack can be used as secondary option. Depending on the distance from the EPS to the NanoDock SDR in the stack the voltage loss varies quite a bit. This can be mitigated by using more pins, so the current and voltage are within limits.

The GPS heartbeat (H1 Pin 2) is connected via a resistor divider to the 1.8V FPGA pin "IO_L13P_T2_MRCC_13" ball AD20.

2.1.2 J7 – SD Card

Molex 500873-0806

Pin	Description
1	SDIO_0_IO2 *
2	SDIO_0_IO3 *
3	SDIO_0_CMD *
4	SD_VCC
5	SDIO_0_CLK *
6	GND
7	SDIO_0_IO0 *
8	SDIO_0_IO1 *

* The marked pins are mutually exclusive with marked pins on J12

NanoMind Z7000			NanoDock SDR					Notes
V	Ball	Xc7z030 pin name	Pin	to	Pin	SD Card	V	
3.3V	C18	PS_MIO45_501	J3-18		J7-2	SDIO_0_IO3	3.3V	Mutually exclusive with J12-6
3.3V	E18	PS_MIO44_501	J3-20		J7-1	SDIO_0_IO2	3.3V	Mutually exclusive with J12-7
3.3V	D18	PS_MIO43_501	J3-22		J7-8	SDIO_0_IO1	3.3V	Mutually exclusive with J12-4
3.3V	F17	PS_MIO42_501	J3-24		J7-7	SDIO_0_IO0	3.3V	Mutually exclusive with J12-3
3.3V	C19	PS_MIO41_501	J3-26		J7-3	SDIO_0_CMD	3.3V	Mutually exclusive with J12-5
3.3V	C22	PS_MIO40_501	J3-28		J7-5	SDIO_0_CLK	3.3V	Mutually exclusive with J12-2

2.1.3 J11 – 3.3 V UART

Molex PicoBlade 1.25 mm Pitch. 53261-0471.

Pin	Description
1	GND
2	n.c.
3	ARM_UART0_RX
4	ARM_UART0_TX

NanoMind Z7000			NanoDock SDR					Notes
V	Ball	Xc7z030 pin name	Pin	to	Pin	UART0	V	
GND			GND		J11-1	GND	GND	
-	-	-	-		J11-2	-	-	Not used
3.3V	D23	PS_MIO14_500	J3-91		J11-3	UART0 RX	3.3V	PS UART input
3.3V	C24	PS_MIO15_500	J3-86		J11-4	UART0 TX	3.3V	PS UART output

2.1.4 J14 – USB

Pin	Description
1	VBUS
2	USB_N
3	USB_P
4	OTG_ID
5	GND

NanoMind Z7000			NanoDock SDR					Notes
V	Ball	Xc7z030 pin name	Pin	to	Pin	USB 2.0	V	
Occupies PS_MIO28_501 to PS_MIO39_501 for USB0 PHY interface			J2-56		J14-1	USB_VBUS	5.0V	
			J2-50		J14-2	USB_N	5.0V	
			J2-48		J14-3	USB_P	5.0V	
			J2-52		J14-4	OTG_ID	5.0V	
GND			GND		J14-5	GND	GND	

2.1.5 J15 – RS422

Molex PicoBlade 1.25 mm Pitch. 53261-0671.

Pin	Description
1	TX_N
2	TX_P
3	GND
4	n.a.
5	RX_N with 120 Ω onboard termination
6	RX_P with 120 Ω onboard termination

NanoMind Z7000			NanoDock SDR					Notes
V	Ball	Xc7z030 pin name	Pin	to	Pin	RS422	V	
3.3V	F19	PS_MIO25_501	J3-19		U8-2	Not applicable	3.3V	PS UART1 is connected to the RS-422 transceiver
3.3V	J19	PS_MIO24_501	J3-17		U8-3		3.3V	
Not applicable			U8-6		J15-1	TX_N	3V max VOC	RS-422 Differential output
			U8-5		J15-2	TX_P		
			-		J15-3	NA	3.3V	Reserved for internal use.
			GND		J15-4	GND	GND	
			U8-7		J15-5	RX_N	-7V ≤ V ≤ 12V	RS-422 Differential Input - Terminated with 120 Ohm
			U8-8		J15-6	RX_P		

2.1.6 J16 – EPS

Molex PicoLock 1.50 mm Pitch. 504050-0691.

Pin	Description
1	VCC
2	VCC
3	VCC
4	GND
5	GND
6	GND

NanoMind Z7000			NanoDock SDR					Notes
V	Ball	Xc7z030 pin name	Pin	to	Pin	Power supply	V	
Not Applicable					J16-1	5.0V @ 2A	5.0V	Recommended power supply input connector
					J16-2			
					J16-3			
					J16-4	GND	GND	Recommended Ground input connector
					J16-5			
					J16-6			

2.1.7 J20 – I2C

Molex PicoBlade 1.25 mm Pitch. 53261-0471.

Pin	Description
1	ARM_SCL0 has 200k Ω pull-up resistor to 3.3 V.
2	ARM_SDA0 has 200k Ω pull-up resistor to 3.3 V.
3	3.3 V Supply Output
4	GND

NanoMind Z7000			NanoDock SDR					Notes
V	Ball	Xc7z030 pin name	Pin	to	Pin	I2C 0	V	
3.3V	H17	PS_MIO26_501	J3-21		J20-1	SCL0	3.3V	
3.3V	F18	PS_MIO27_501	J3-23		J20-2	SDA0	3.3V	
-	-	-			J20-3	NA	3.3V	Reserved for internal use
-	-	-			J20-4	GND	GND	

2.1.8 J22 – Expansion

Molex PicoLock 1.50 mm Pitch. 504050-0491.

Pin	Description
1	GND
2	CANL
3	CANH
4	VCC

NanoMind Z7000			NanoDock SDR					Notes
V	Ball	Xc7z030 pin name	Pin	to	Pin	CAN BUS	V	
3.3V	A23	PS_MIO12_500	J3-100	-	-	CAN_TX	3.3V	
3.3V	B25	PS_MIO13_500	J3-98	-	-	CAN_RX	3.3V	
3.3V	G22	PS_MIO22_501	J3-13	-	-	CAN_Rs	3.3V	Mutually exclusive with J12-9
-	-	-	-	-	J22-1	GND	GND	
-	-	-	-	-	J22-2	CAN_N		Differential Input
-	-	-	-	-	J22-3	CAN_P		
-	-	-	-	-	J22-4	5.0V @ 1.5A	5.0V	This pin is shorted to J16-1 to J16-3

2.2 Slot A

NanoMind Z7000			NanoDock SDR			NanoCom TR-600 Slot A			Notes
V	**Ball**	**Xc7z030 pin name**	**Pin**	**to**	**Pin**	**AD9361 pin name**	**Ball**	**V**	
1.8V	E15	IO_L14N_T2_AD4N_SRCC_35	J3-70		J4-53	P0_D0/TX_D0_N	E12	1.8V	Dedicated Pin
1.8V	F15	IO_L14P_T2_AD4P_SRCC_35	J3-72		J4-55	P0_D1/TX_D0_P	D11	1.8V	Dedicated Pin
1.8V	C13	IO_L19N_T3_VREF_35	J3-76		J4-59	P0_D2/TX_D1_N	E11	1.8V	Dedicated Pin
1.8V	D13	IO_L19P_T3_35	J3-78		J4-61	P0_D3/TX_D1_P	D10	1.8V	Dedicated Pin
1.8V	E13	IO_L6N_T0_VREF_35	J3-82		J4-65	P0_D4/TX_D2_N	E10	1.8V	Dedicated Pin
1.8V	F13	IO_L6P_T0_35	J3-84		J4-67	P0_D5/TX_D2_P	D9	1.8V	Dedicated Pin
1.8V	D16	IO_L16N_T2_35	J3-85		J4-71	P0_D6/TX_D3_N	E9	1.8V	Dedicated Pin
1.8V	E16	IO_L16P_T2_35	J3-87		J4-73	P0_D7/TX_D3_P	D8	1.8V	Dedicated Pin
1.8V	A17	IO_L18N_T2_AD13N_35	J3-93		J4-77	P0_D8/TX_D4_N	E8	1.8V	Dedicated Pin
1.8V	B17	IO_L18P_T2_AD13P_35	J3-95		J4-79	P0_D9/TX_D4_P	D7	1.8V	Dedicated Pin
1.8V	B15	IO_L17N_T2_AD5N_35	J3-97		J4-83	P0_D10/TX_D5_N	F8	1.8V	Dedicated Pin
1.8V	B16	IO_L17P_T2_AD5P_35	J3-99		J4-85	P0_D11/TX_D5_P	E7	1.8V	Dedicated Pin
1.8V	D6	IO_L14P_T2_SRCC_34	J1-13		J5-44	P1_D1/RX_D0_P	J12	1.8V	Dedicated Pin
1.8V	C6	IO_L14N_T2_SRCC_34	J1-15		J5-46	P1_D0/RX_D0_N	K11	1.8V	Dedicated Pin
1.8V	A9	IO_L17P_T2_34	J1-12		J5-50	P1_D3/RX_D1_P	J11	1.8V	Dedicated Pin
1.8V	A8	IO_L17N_T2_34	J1-14		J5-52	P1_D2/RX_D1_N	K10	1.8V	Dedicated Pin
1.8V	C8	IO_L13P_T2_MRCC_34	J1-16		J5-56	P1_D5/RX_D2_P	J10	1.8V	Dedicated Pin
1.8V	C7	IO_L13N_T2_MRCC_34	J1-18		J5-58	P1_D4/RX_D2_N	K9	1.8V	Dedicated Pin
1.8V	F5	IO_L7P_T1_34	J1-22		J5-62	P1_D7/RX_D3_P	J9	1.8V	Dedicated Pin
1.8V	E5	IO_L7N_T1_34	J1-24		J5-64	P1_D6/RX_D3_N	K8	1.8V	Dedicated Pin
1.8V	D9	IO_L8P_T1_34	J1-26		J5-68	P1_D9/RX_D4_P	J8	1.8V	Dedicated Pin
1.8V	D8	IO_L8N_T1_34	J1-28		J5-70	P1_D8/RX_D4_N	K7	1.8V	Dedicated Pin
1.8V	G7	IO_L12P_T1_MRCC_34	J1-32		J5-74	P1_D11/RX_D5_P	H8	1.8V	Dedicated Pin
1.8V	F7	IO_L12N_T1_MRCC_34	J1-34		J5-76	P1_D10/RX_D5_N	J7	1.8V	Dedicated Pin
1.8V	H7	IO_L4P_T0_34	J1-36		J5-80	RX_FRAME_P	G8	1.8V	Dedicated Pin
1.8V	H6	IO_L4N_T0_34	J1-38		J5-82	RX_FRAME_N	G7	1.8V	Dedicated Pin
1.8V	B7	IO_L18P_T2_34	J1-21		J5-38	DATA_CLK_P	G11	1.8V	Dedicated Pin
1.8V	A7	IO_L18N_T2_34	J1-23		J5-40	DATA_CLK_N	H11	1.8V	Dedicated Pin
1.8V	D14	IO_L13N_T2_MRCC_35	J3-59		J4-33	TX_FRAME_N	H9	1.8V	Dedicated Pin
1.8V	D15	IO_L13P_T2_MRCC_35	J3-61		J4-35	TX_FRAME_P	G9	1.8V	Dedicated Pin
1.8V	B11	IO_L23N_T3_35	J3-66		J4-39	FB_CLK_N	G10	1.8V	Dedicated Pin
1.8V	C11	IO_L23P_T3_35	J3-68		J4-41	FB_CLK_P	F10	1.8V	Dedicated Pin
1.8V	AC22	IO_L14N_T2_SRCC_13	J1-73		J5-69	SPI_ENB	K6	1.8V	Dedicated Pin
1.8V	AF20	IO_L15N_T2_DQS_13	J1-53		J5-45	PG_FMC	na	1.8V	Dedicated Pin
1.8V	AE21	IO_L16N_T2_13	J1-63		J4-25	SDA	na	1.8V	Shared Pin between Slot A, B and C
1.8V	AE20	IO_L16P_T2_13	J1-61		J4-29	SCL	na	1.8V	Shared Pin between Slot A, B and C
1.8V	AA20	IO_L20P_T3_13	J1-35		J4-17	ADC_IRQ	na	1.8V	Dedicated Pin
1.8V	AC18	IO_L21P_T3_DQS_13	J1-41		J5-37	Fc_CTL_ext	na	1.8V	Dedicated Pin
1.8V	AD19	IO_L17N_T2_13	J1-47		J5-41	SYNC	na	1.8V	Shared Pin between Slot A, B and C

1.8V	AC21	IO_L14P_T2_SRCC_13	J1-71		J5-57	ENABLE	G6	1.8V	Dedicated Pin
1.8V	AF19	IO_L15P_T2_DQS_13	J1-51		J5-61	SYNC_IN	H5	1.8V	Shared Pin between Slot A, B and C
1.8V	AF23	IO_L8N_T1_13	J1-84		J5-73	SPI_DO	L6	1.8V	Shared Pin between Slot A, B and C
1.8V	AB24	IO_L6N_T0_VREF_13	J1-77		J5-77	RESETB	K5	1.8V	Shared Pin between Slot A, B and C
1.8V	AD25	IO_L4P_T0_13	J1-81		J5-81	SPI_CLK	J5	1.8V	Shared Pin between Slot A, B and C
1.8V	AE26	IO_L3N_T0_DQS_13	J1-93		J5-89	SPI_DI	J4	1.8V	Shared Pin between Slot A, B and C
1.8V	AF25	IO_L5N_T0_13	J1-97		J5-93	TXNRX	H4	1.8V	Dedicated Pin
1.8V	AE22	IO_L7P_T1_13	J1-85		J5-97	EN_AGC	G5	1.8V	Dedicated Pin

2.3 NanoDock SDR Bottom

The connectors of the bottom side of the NanoDock SDR are shown in Fig. 2-2.

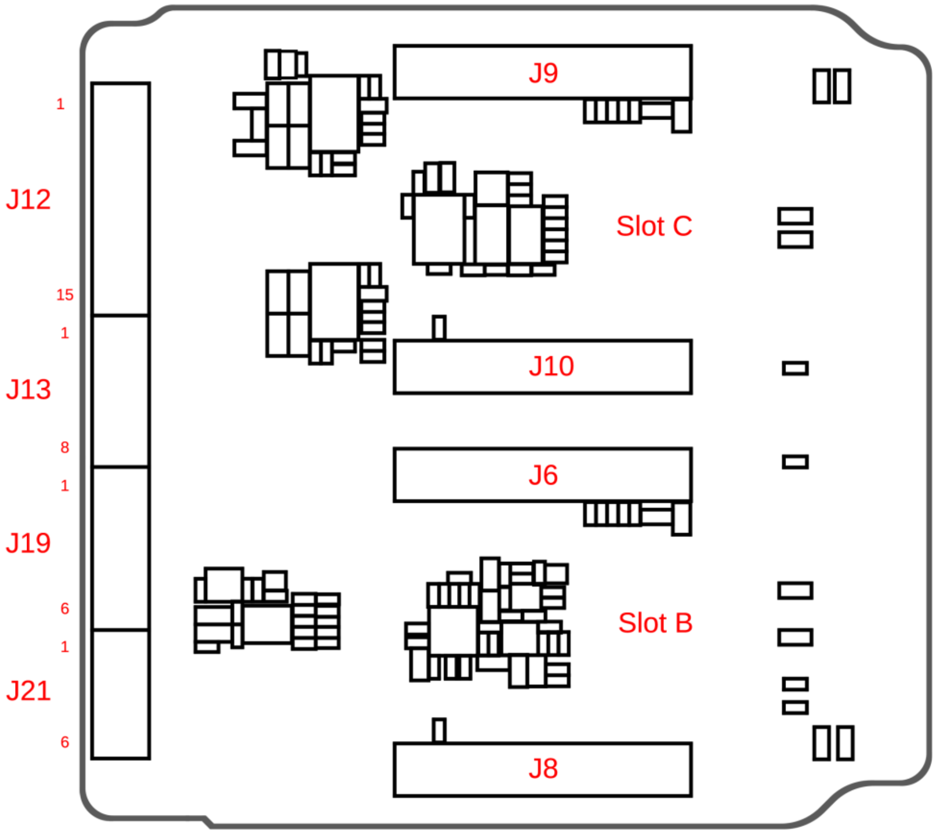


Fig. 2-2 NanoDock SDR (bottom)

2.3.1 J12 – 3.3 V Single-ended

Molex PicoBlade 1.25 mm Pitch. 53261-1571. J12 and J7 (SD card) use the same signals so they are mutually exclusive.

Pin	Description
1	PCA-P2
2	SDIO_0_CLK *
3	SDIO_0_IO0 *
4	SDIO_0_IO1 *
5	SDIO_0_CMD *
6	SDIO_0_IO3 *
7	SDIO_0_IO2 *
8	MIO23
9	CAN_Rs
10	MOI9
11	NanoDock EN has 143k Ω pull-up resistor to VCC **
12	MIO19
13	MOI0
14	3.3V_MB
15	GND

* The marked pins are mutually exclusive with marked pins on J7
** By pulling the signal low the NanoDock SDR and its daughterboards are turned off

NanoMind Z7000			NanoDock SDR					Notes
V	Ball	Xc7z030 pin name	Pin	to	Pin	PS expansion IO	V	
-	-	-	-		J12-1	PCA-P2	3.3V	Mutually exclusive with SD-card support on J7
3.3V	C22	PS_MIO40_501	J3-28		J12-2	SDIO_0_CLK	3.3V	
3.3V	F17	PS_MIO42_501	J3-24		J12-3	SDIO_0_IO0	3.3V	
3.3V	D18	PS_MIO43_501	J3-22		J12-4	SDIO_0_IO1	3.3V	
3.3V	C19	PS_MIO41_501	J3-26		J12-5	SDIO_0_CMD	3.3V	
3.3V	C18	PS_MIO45_501	J3-18		J12-6	SDIO_0_IO3	3.3V	
3.3V	E18	PS_MIO44_501	J3-20		J12-7	SDIO_0_IO2	3.3V	
3.3V	F20	PS_MIO23_501	J3-15		J12-8	MIO23	3.3V	Free to use
3.3V	G22	PS_MIO22_501	J3-13		J12-9	CAN_Rs	3.3V	Mutually exclusive with CAN RS control
3.3V	D24	PS_MIO9_500	J3-92		J12-10	MOI9	3.3V	Mutually exclusive with PL SW supply control
-	-	-	-		J12-11	NanoDock EN	5.0V	Above 1.8V = ON (pull-up 124Kohm to 5.0V)
3.3V	G19	PS_MIO19_501	J3-7		J12-12	MIO19	3.3V	Free to used
3.3V	E26	PS_MIO0_500	J3-88		J12-13	MOI0	3.3V	Mutually exclusive with USB phy suspend
3.3V	Z7000 supply input		J1-1		J12-14	3.3V_MB	3.3V	
GND			GND		J12-15	GND	GND	

2.3.2 J13 – JTAG

Molex PicoBlade 1.25 mm Pitch. 53261-0871.

Pin	Description
1	JTAG_TD0
2	JTAG_TCK
3	JTAG_TMS
4	JTAG_TDI
5	PB_SRST_B
6	PB_SRST_B
7	3.3 V Supply output
8	GND

NanoMind Z7000			NanoDock SDR					Notes
V	Ball	Xc7z030 pin name	Pin	to	Pin	JTAG	V	
3.3V	W10	TDO_0	J1-98		J13-1	JTAG_TDO	3.3V	
3.3V	W12	TCK_0	J1-100		J13-2	JTAG_TCK	3.3V	
3.3V	W11	TMS_0	J1-94		J13-3	JTAG_TMS	3.3V	
3.3V	V11	TDI_0	J1-96		J13-4	JTAG_TDI	3.3V	
3.3V	A22	PS_SRST_B_501	J1-17		J13-5	PS_SRST_B	3.3V	
3.3V	A22	PS_SRST_B_501	J1-17		J13-6	PS_SRST_B	3.3V	
3.3V	PS supply output		J1-9		J13-7	3.3V_PS	3.3V	
GND			GND		J13-8	GND	GND	

2.3.3 J19 – 1.8 V LVDS/Single-ended

Molex PicoBlade 1.25 mm Pitch. 53261-0971.

Pin	Description
1	L9_P_13 1.8V single-ended
2	L9_N_13 1.8V single-ended
3	L1_P_13 1.8V single-ended
4	L1_N_13 1.8V single-ended
5	GND
6	L20_N_33
7	L20_P_33
8	L22_N_33
9	L22_P_33

NanoMind Z7000			NanoDock SDR					Notes
V	Ball	Xc7z030 pin name	Pin	to	Pin	PL expansion IO	V	
1.8V	AB21	IO_L9P_T1_DQS_13	J1-66		J19-1	L9_P_13	1.8V	Free to use
1.8V	AB22	IO_L9N_T1_DQS_13	J1-68		J19-2	L9_N_13	1.8V	Free to use
1.8V	AA25	IO_L1P_T0_13	J1-76		J19-3	L1_P_13	1.8V	Free to use
1.8V	AB25	IO_L1N_T0_13	J1-78		J19-4	L1_N_13	1.8V	Free to use
GND			GND		GND	GND	GND	Free to use
1.8V	J5	IO_L20N_T3_33	J2-33		J19-6	L20_N_33	1.8V	Free to use
1.8V	K5	IO_L20P_T3_33	J2-31		J19-7	L20_P_33	1.8V	Free to use
1.8V	J6	IO_L22N_T3_33	J2-27		J19-8	L22_N_33	1.8V	Free to use
1.8V	K6	IO_L22P_T3_33	J2-25		J19-9	L22_P_33	1.8V	Free to use

2.3.4 J21 – 1.8 V Single-ended

Molex PicoBlade 1.25 mm Pitch. 53261-0671.

Pin	Description
1	L18_N_13, 1.8V single-ended
2	L18_P_13, 1.8V single-ended
3	L23_N_13, 1.8V single-ended
4	L23_P_13, 1.8V single-ended
5	L24_N_13, 1.8V single-ended
6	L24_P_13, 1.8V single-ended

NanoMind Z7000			NanoDock SDR					Notes
V	Ball	Xc7z030 pin name	Pin	to	Pin	PL expansion IO - 1	V	
1.8V	AF18	IO_L18N_T2_13	J1-58		J21-1	L18_N_13	1.8V	Free to use
1.8V	AE18	IO_L18P_T2_13	J1-56		J21-2	L18_P_13	1.8V	Free to use
1.8V	W19	IO_L23N_T3_13	J1-54		J21-3	L23_N_13	1.8V	Free to use
1.8V	W18	IO_L23P_T3_13	J1-52		J21-4	L23_P_13	1.8V	Free to use
1.8V	AA18	IO_L24N_T3_13	J1-48		J21-5	L24_N_13	1.8V	Free to use
1.8V	Y18	IO_L24P_T3_13	J1-46		J21-6	L24_P_13	1.8V	Free to use

2.3.5 Slot B

NanoMind Z7000			NanoDock SDR			NanoCom TR-600 Slot B			Notes
V	Ball	Xc7z030 pin name	Pin	to	Pin	AD9361 pin name	Ball	V	
1.8V	D10	IO_L2N_T0_AD8N_35	J3-36		J6-53	P0_D0/TX_D0_N	E12	1.8V	Dedicated Pin
1.8V	E10	IO_L2P_T0_AD8P_35	J3-38		J6-55	P0_D1/TX_D0_P	D11	1.8V	Dedicated Pin
1.8V	F14	IO_L11N_T1_SRCC_35	J3-42		J6-59	P0_D2/TX_D1_N	E11	1.8V	Dedicated Pin
1.8V	G14	IO_L11P_T1_SRCC_35	J3-44		J6-61	P0_D3/TX_D1_P	D10	1.8V	Dedicated Pin
1.8V	B12	IO_L22N_T3_AD7N_35	J3-46		J6-65	P0_D4/TX_D2_N	E10	1.8V	Dedicated Pin
1.8V	C12	IO_L22P_T3_AD7P_35	J3-48		J6-67	P0_D5/TX_D2_P	D9	1.8V	Dedicated Pin
1.8V	J13	IO_L8N_T1_AD10N_35	J3-50		J6-71	P0_D6/TX_D3_N	E9	1.8V	Dedicated Pin
1.8V	K13	IO_L8P_T1_AD10P_35	J3-52		J6-73	P0_D7/TX_D3_P	D8	1.8V	Dedicated Pin
1.8V	G11	IO_L5N_T0_AD9N_35	J3-56		J6-77	P0_D8/TX_D4_N	E8	1.8V	Dedicated Pin
1.8V	G12	IO_L5P_T0_AD9P_35	J3-58		J6-79	P0_D9/TX_D4_P	D7	1.8V	Dedicated Pin
1.8V	F10	IO_L3N_T0_DQS_AD1N_35	J3-60		J6-83	P0_D10/TX_D5_N	F8	1.8V	Dedicated Pin
1.8V	G10	IO_L3P_T0_DQS_AD1P_35	J3-62		J6-85	P0_D11/TX_D5_P	E7	1.8V	Dedicated Pin
1.8V	M8	IO_L21P_T3_DQS_33	J2-14		J8-44	P1_D1/RX_D0_P	J12	1.8V	Dedicated Pin
1.8V	L8	IO_L21N_T3_DQS_33	J2-16		J8-46	P1_D0/RX_D0_N	K11	1.8V	Dedicated Pin
1.8V	N1	IO_L18P_T2_33	J2-19		J8-50	P1_D3/RX_D1_P	J11	1.8V	Dedicated Pin
1.8V	M1	IO_L18N_T2_33	J2-21		J8-52	P1_D2/RX_D1_N	K10	1.8V	Dedicated Pin
1.8V	N3	IO_L15P_T2_DQS_33	J2-20		J8-56	P1_D5/RX_D2_P	J10	1.8V	Dedicated Pin
1.8V	N2	IO_L15N_T2_DQS_33	J2-22		J8-58	P1_D4/RX_D2_N	K9	1.8V	Dedicated Pin
1.8V	N4	IO_L17P_T2_33	J2-13		J8-62	P1_D7/RX_D3_P	J9	1.8V	Dedicated Pin
1.8V	M4	IO_L17N_T2_33	J2-15		J8-64	P1_D6/RX_D3_N	K8	1.8V	Dedicated Pin
1.8V	L5	IO_L14P_T2_SRCC_33	J2-26		J8-68	P1_D9/RX_D4_P	J8	1.8V	Dedicated Pin
1.8V	L4	IO_L14N_T2_SRCC_33	J2-28		J8-70	P1_D8/RX_D4_N	K7	1.8V	Dedicated Pin
1.8V	N7	IO_L23P_T3_33	J2-7		J8-74	P1_D11/RX_D5_P	H8	1.8V	Dedicated Pin
1.8V	N6	IO_L23N_T3_33	J2-9		J8-76	P1_D10/RX_D5_N	J7	1.8V	Dedicated Pin
1.8V	J4	IO_L12P_T1_MRCC_33	J2-32		J8-80	RX_FRAME_P	G8	1.8V	Dedicated Pin
1.8V	J3	IO_L12N_T1_MRCC_33	J2-34		J8-82	RX_FRAME_N	G7	1.8V	Dedicated Pin
1.8V	M6	IO_L13P_T2_MRCC_33	J2-8		J8-38	DATA_CLK_P	G11	1.8V	Dedicated Pin
1.8V	M5	IO_L13N_T2_MRCC_33	J2-10		J8-40	DATA_CLK_N	H11	1.8V	Dedicated Pin
1.8V	E12	IO_L1N_T0_AD0N_35	J3-32		J6-33	TX_FRAME_N	H9	1.8V	Dedicated Pin
1.8V	F12	IO_L1P_T0_AD0P_35	J3-34		J6-35	TX_FRAME_P	G9	1.8V	Dedicated Pin
1.8V	D11	IO_L4N_T0_35	J3-35		J6-39	FB_CLK_N	G10	1.8V	Dedicated Pin
1.8V	E11	IO_L4P_T0_35	J3-37		J6-41	FB_CLK_P	F10	1.8V	Dedicated Pin
1.8V	AD23	IO_L11P_T1_SRCC_13	J1-65		J8-69	SPI_ENB	K6	1.8V	Dedicated Pin
1.8V	AA19	IO_L22P_T3_13	J1-31		J8-45	PG_FMC	na	1.8V	Dedicated Pin
1.8V	AE21	IO_L16N_T2_13	J1-63		J6-25	SDA	na	1.8V	Shared Pin between Slot A, B and C
1.8V	AE20	IO_L16P_T2_13	J1-61		J6-29	SCL	na	1.8V	Shared Pin between Slot A, B and C
1.8V	AB19	IO_L22N_T3_13	J1-33		J6-17	ADC_IRQ	na	1.8V	Dedicated Pin
1.8V	AD18	IO_L17P_T2_13	J1-45		J8-37	Fc_CTL_ext	na	1.8V	Dedicated Pin
1.8V	AD19	IO_L17N_T2_13	J1-47		J8-41	SYNC	na	1.8V	Shared Pin between Slot A, B and C

1.8V	AA22	IO_L10P_T1_13	J1-55		J8-57	ENABLE	G6	1.8V	Dedicated Pin
1.8V	AF19	IO_L15P_T2_DQS_13	J1-51		J8-61	SYNC_IN	H5	1.8V	Shared Pin between Slot A, B and C
1.8V	AF23	IO_L8N_T1_13	J1-84		J8-73	SPI_DO	L6	1.8V	Shared Pin between Slot A, B and C
1.8V	AB24	IO_L6N_T0_VREF_13	J1-77		J8-77	RESETB	K5	1.8V	Shared Pin between Slot A, B and C
1.8V	AD25	IO_L4P_T0_13	J1-81		J8-81	SPI_CLK	J5	1.8V	Shared Pin between Slot A, B and C
1.8V	AE26	IO_L3N_T0_DQS_13	J1-93		J8-89	SPI_DI	J4	1.8V	Shared Pin between Slot A, B and C
1.8V	AE25	IO_L3P_T0_DQS_13	J1-91		J8-93	TXNRX	H4	1.8V	Dedicated Pin
1.8V	AF24	IO_L5P_T0_13	J1-95		J8-97	EN_AGC	G5	1.8V	Dedicated Pin

2.3.6 Slot C

NanoMind Z7000			NanoDock SDR			NanoCom TR-600 Slot C			Notes
V	**Ball**	**Xc7z030 pin name**	**Pin**	**to**	**Pin**	**AD9361 pin name**	**Ball**	**V**	
1.8V	E1	IO_L5N_T0_33	J2-39		J9-53	P0_D0/TX_D0_N	E12	1.8V	Dedicated Pin
1.8V	E2	IO_L5P_T0_33	J2-37		J9-55	P0_D1/TX_D0_P	D11	1.8V	Dedicated Pin
1.8V	G1	IO_L10N_T1_33	J2-60		J9-59	P0_D2/TX_D1_N	E11	1.8V	Dedicated Pin
1.8V	H2	IO_L10P_T1_33	J2-58		J9-61	P0_D3/TX_D1_P	D10	1.8V	Dedicated Pin
1.8V	F4	IO_L1N_T0_33	J2-49		J9-65	P0_D4/TX_D2_N	E10	1.8V	Dedicated Pin
1.8V	G4	IO_L1P_T0_33	J2-47		J9-67	P0_D5/TX_D2_P	D9	1.8V	Dedicated Pin
1.8V	H1	IO_L7N_T1_33	J2-43		J9-71	P0_D6/TX_D3_N	E9	1.8V	Dedicated Pin
1.8V	J1	IO_L7P_T1_33	J2-41		J9-73	P0_D7/TX_D3_P	D8	1.8V	Dedicated Pin
1.8V	K1	IO_L9N_T1_DQS_33	J2-44		J9-77	P0_D8/TX_D4_N	E8	1.8V	Dedicated Pin
1.8V	K2	IO_L9P_T1_DQS_33	J2-42		J9-79	P0_D9/TX_D4_P	D7	1.8V	Dedicated Pin
1.8V	H3	IO_L8N_T1_33	J2-40		J9-83	P0_D10/TX_D5_N	F8	1.8V	Dedicated Pin
1.8V	H4	IO_L8P_T1_33	J2-38		J9-85	P0_D11/TX_D5_P	E7	1.8V	Dedicated Pin
1.8V	K15	IO_L9P_T1_DQS_AD3P_35	J3-47		J10-44	P1_D1/RX_D0_P	J12	1.8V	Dedicated Pin
1.8V	J15	IO_L9N_T1_DQS_AD3N_35	J3-45		J10-46	P1_D0/RX_D0_N	K11	1.8V	Dedicated Pin
1.8V	C14	IO_L20P_T3_AD6P_35	J3-51		J10-50	P1_D3/RX_D1_P	J11	1.8V	Dedicated Pin
1.8V	B14	IO_L20N_T3_AD6N_35	J3-49		J10-52	P1_D2/RX_D1_N	K10	1.8V	Dedicated Pin
1.8V	G16	IO_L10P_T1_AD11P_35	J3-57		J10-56	P1_D5/RX_D2_P	J10	1.8V	Dedicated Pin
1.8V	G15	IO_L10N_T1_AD11N_35	J3-55		J10-58	P1_D4/RX_D2_N	K9	1.8V	Dedicated Pin
1.8V	A13	IO_L24P_T3_AD15P_35	J3-67		J10-62	P1_D7/RX_D3_P	J9	1.8V	Dedicated Pin
1.8V	A12	IO_L24N_T3_AD15N_35	J3-65		J10-64	P1_D6/RX_D3_N	K8	1.8V	Dedicated Pin
1.8V	C17	IO_L15P_T2_DQS_AD12P_35	J3-71		J10-68	P1_D9/RX_D4_P	J8	1.8V	Dedicated Pin
1.8V	C16	IO_L15N_T2_DQS_AD12N_35	J3-69		J10-70	P1_D8/RX_D4_N	K7	1.8V	Dedicated Pin
1.8V	A15	IO_L21P_T3_DQS_AD14P_35	J3-77		J10-74	P1_D11/RX_D5_P	H8	1.8V	Dedicated Pin
1.8V	A14	IO_L21N_T3_DQS_AD14N_35	J3-75		J10-76	P1_D10/RX_D5_N	J7	1.8V	Dedicated Pin
1.8V	J14	IO_L12P_T1_MRCC_35	J3-81		J10-80	RX_FRAME_P	G8	1.8V	Dedicated Pin
1.8V	H14	IO_L12N_T1_MRCC_35	J3-79		J10-82	RX_FRAME_N	G7	1.8V	Dedicated Pin

1.8V	H13	IO_L7P_T1_AD2P_35	J3-41		J10-38	DATA_CLK_P	G11	1.8V	Dedicated Pin
1.8V	H12	IO_L7N_T1_AD2N_35	J3-39		J10-40	DATA_CLK_N	H11	1.8V	Dedicated Pin
1.8V	D3	IO_L2N_T0_33	J2-53		J9-33	TX_FRAME_N	H9	1.8V	Dedicated Pin
1.8V	D4	IO_L2P_T0_33	J2-51		J9-35	TX_FRAME_P	G9	1.8V	Dedicated Pin
1.8V	C1	IO_L4N_T0_33	J2-59		J9-39	FB_CLK_N	G10	1.8V	Dedicated Pin
1.8V	D1	IO_L4P_T0_33	J2-57		J9-41	FB_CLK_P	F10	1.8V	Dedicated Pin
1.8V	AA24	IO_L6P_T0_13	J1-75		J10-69	SPI_ENB	K6	1.8V	Dedicated Pin
1.8V	AA23	IO_L10N_T1_13	J1-57		J10-45	PG_FMC	na	1.8V	Dedicated Pin
1.8V	AE21	IO_L16N_T2_13	J1-63		J9-25	SDA	na	1.8V	Shared Pin between Slot A, B and C
1.8V	AE20	IO_L16P_T2_13	J1-61		J9-29	SCL	na	1.8V	Shared Pin between Slot A, B and C
1.8V	AB20	IO_L20N_T3_13	J1-37		J9-17	ADC_IRQ	na	1.8V	Dedicated Pin
1.8V	AC19	IO_L21N_T3_DQS_13	J1-43		J10-37	Fc_CTL_ext	na	1.8V	Dedicated Pin
1.8V	AD19	IO_L17N_T2_13	J1-47		J10-41	SYNC	na	1.8V	Shared Pin between Slot A, B and C
1.8V	AD24	IO_L11N_T1_SRCC_13	J1-67		J10-57	ENABLE	G6	1.8V	Dedicated Pin
1.8V	AF19	IO_L15P_T2_DQS_13	J1-51		J10-61	SYNC_IN	H5	1.8V	Shared Pin between Slot A, B and C
1.8V	AF23	IO_L8N_T1_13	J1-84		J10-73	SPI_DO	L6	1.8V	Shared Pin between Slot A, B and C
1.8V	AB24	IO_L6N_T0_VREF_13	J1-77		J10-77	RESETB	K5	1.8V	Shared Pin between Slot A, B and C
1.8V	AD25	IO_L4P_T0_13	J1-81		J10-81	SPI_CLK	J5	1.8V	Shared Pin between Slot A, B and C
1.8V	AE26	IO_L3N_T0_DQS_13	J1-93		J10-89	SPI_DI	J4	1.8V	Shared Pin between Slot A, B and C
1.8V	AD26	IO_L4N_T0_13	J1-83		J10-93	TXNRX	H4	1.8V	Dedicated Pin
1.8V	AF22	IO_L7N_T1_13	J1-87		J10-97	EN_AGC	G5	1.8V	Dedicated Pin

2.4 NanoMind Z7000

The Z7000 is connected to the SDR Dock through 2x 100 pin Samtec and the 1x Samtec LSHM-130-04.0-L-DV-A-S-K-TR connectors – see Fig. 2-3. The Z7000 is powered through the SDR Dock.

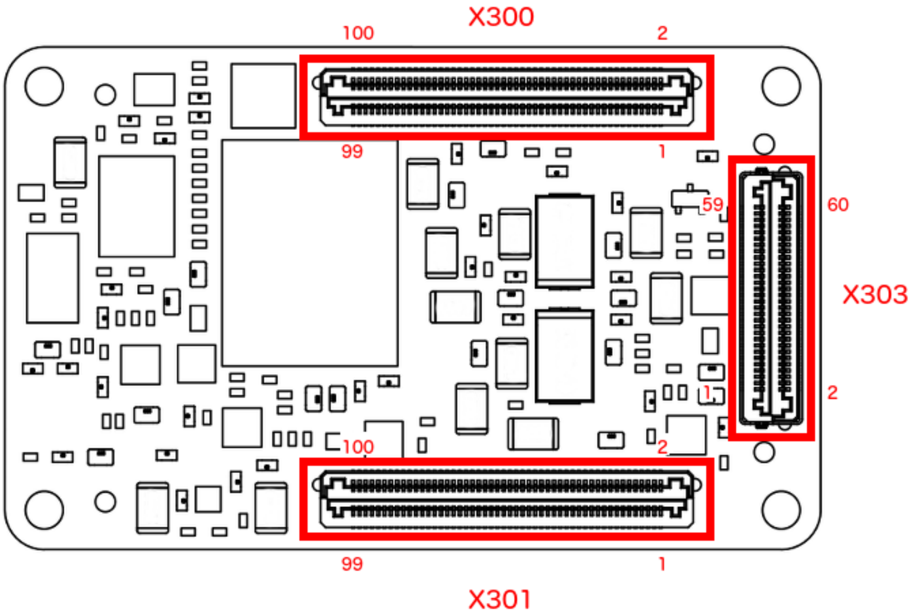


Fig. 2-3 Z7000 X300, X301 and X303 Connectors

2.4.1 X303, X300 and X303

The description of these three connectors are not normally handed out to customers. Please contact GomSpace support for further information.

2.5 NanoCom TR-600

The TR-600 is connected to the SDR Dock through 2x 100 pin Samtec connectors. The TR-600 is powered through the SDR Dock.

The image below shows the top side of the TR-600, under the shield.

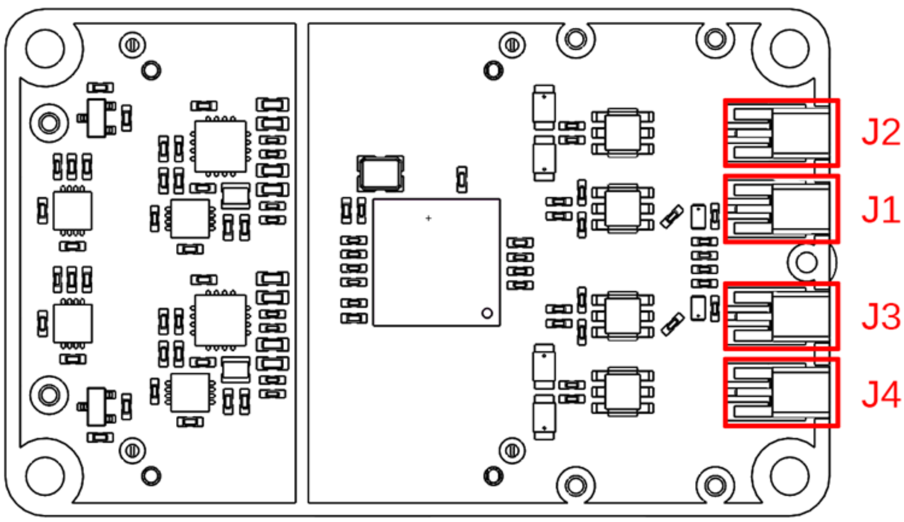


Fig. 2-4 TR-600 top side connectors

2.5.1 J1 – Rx 1

Molex SSMCX EDGE 73415-4670.

Pin	Description
1	Rx 1
2	GND

2.5.2 J2 – Tx 1

Pin	Description
1	Tx 1
2	GND

2.5.3 J3 – Rx 2

Molex SSMCX EDGE 73415-4670.

Pin	Description
1	Rx 2
2	GND

2.5.4 J4 – Tx 2

Molex SSMCX EDGE 73415-4670.

Pin	Description
1	Tx 2
2	GND

2.5.5 X1 and X2

The description of these two connectors are not normally handed out to customers. Please contact GomSpace support for further information.

2.5.6 Time Sync

A time sync signal can be received through a connector pin on one of the Samtec connectors. As an example, J12 pin 12 can be used and be configured to 3.3 V or 1.8 V LVCMOS.

3 Interfaces and Protocols

3.1 Electrical Interfaces

The NanoCom SDR supports the following electrical interfaces:

- CAN
- I^2C
- RS422
- LVDS (TR-600)
- USB

3.1.1 LVDS

The RX/TX I and Q data are sent/received over a 12 bit LVDS interface (LVDS 6-bit TX differential input bus with internal LVDS termination + 6-bit RX differential output bus with internal LVDS termination).

3.1.2 USB

The Zynq has two embedded USB controllers of which one is connected to an external phy chip. The board only supports usb peripheral mode, as it can't supply an external device with power.

The reset pin of the USB phy is connected to MIO0 pin of the PS, so this pin needs to be driven high before it is possible to use the USB interface. Note that MIO0 is also used for CAN transceiver mode selection.

3.2 Protocols

3.2.1 CubeSat Space Protocol (CSP)

CSP is a routed network protocol that can be used to transmit data packets between individual subsystems on the satellite bus or between the satellite and ground station. For more information about CSP please read the documentation on libcsp.org.

The CSP network is fully configurable using commands described in the GOSH manual. Contact GomSpace support, if the GOSH manual has not been shipped with the product.

The NanoCom SDR uses the CubeSat Space Protocol (CSP) to transfer data to and from nodes in the CSP network. CSP is supported over:

- CAN
- RS422 (KISS)

The CAN interface on the SDR uses the CSP CAN Fragmentation Protocol (CFP). CFP is a simple method to make CSP packets of up to 256 bytes, span multiple CAN messages of up to 8 bytes each.

If a third party component needs to communicate with one of GomSpace's products, then the easiest way to implement CSP/CFP over CAN is to download the CSP source code from http://libcsp.org and compile the CFP code directly into your own embedded system.

The CAN-bus is connected to each individual module.

3.3 Debug Interface

The NanoDock SDR has a Debug connector (J11), which gives access to the U-Boot bootloader, the Linux kernel shell and the GomSpace shell (GOSH). Through GOSH it is possible to control the Monitor Application. The serial speed is: 115200 bps, 8N1. Please see the GOSH manual for further details.

4 Software

GomSpace's products ship with product specific software and software common for all products. The NanoCom SDR software package consists of:

- SDR SDK
- Csp-client

4.1 SDR SDK

The NanoCom SDR comes with the SDR SDK.

The core of the SDR SDK is HDL code enabling the processing system (PS) to interact with the programmable logic (PL), which in essence enables implementation of custom signal processing utilizing GomSpace's TR-600 radio daughterboards.

The NanoCom SDR SDK includes the components needed for building a Linux distribution for the board and enables you to modify the build. It also includes a reference FPGA design for Vivado, that supports sampling data from a TR-600. See the SDR SDK manual for further details.

The SDR Command & Management SDK is included in the SDR SDK and is described in the NanoCom SDR Sales Document and/or the Software Platform datasheet. These can be downloaded from our web site or by contacting GomSpace Support.

The SDR Command & Management SDK adds services and utilities:

- Parameter Service
- Log Service
- GOSH (GomSpace Shell)
- CSP Library
- FTP Service
- Miscellanies Utilities

4.2 CSP Client

Most of GomSpace's products ship with a client interface called *csp-client*. It contains product specific CSP clients, that enables an OBC, or other CSP network nodes, to communicate with a specific product.

Additionally, *csp-client* contains a scaled down version of *libparam*, including code examples of how to set and get parameter values.

The CSP client for the NanoCom SDR is called *z7000-monitor*.

4.3 Parameter System

Most of GomSpace's products are based on a parameter system implemented in the library *libparam*. It is a lightweight parameter system designed for GomSpace satellite subsystems.

Each product has a number of parameter tables containing specific parameters, which allows for configuration of the product. The parameter tables also include a telemetry table holding state information of the product/system. An example parameter table is shown below.

Address	Name	Type	Description
0x00	param_1	U32	Description of param_1
0x04	param_2	U32	Description of param_2

All the parameter tables and their parameters are described in the product manual. The parameter system allows the parameters to be modified both locally and remotely.

Locally: This enables sending parameter commands directly to a system using GOSH on the debug interface. The command used for accessing parameters locally (param) is described further in the GOSH manual.

Remotely: The parameters of a product can be accessed remotely from other nodes in the CSP network. This can be done either from a GOSH command interface (GOSH running on another hardware product or GOSH running in csp-client/csp-term) or from code using the remote parameter API.

5 Absolute Maximum Ratings

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the SDR. Exposure to absolute maximum rating conditions for extended periods may affect the reliability.

The temperatures of the SDR design is limited by the Zync chip and represents a junction temperature for the FPGA of -40 to 85 °C (Tj).

Symbol	Description	Min.	Max.	Unit
VCC	Supply voltage	4.0	6.5	V
I	Supply current		8.0	A
T_{amb}	Operating temperature	-40	85	°C
$T_{Storage}$	Storage temperature	-40	85	°C

6 Electrical Characteristics

For NanoDock SDR with a NanoMind Z7000, one NanoCom TR-600 and with standard software image idle.

Symbol	Description	Min.	Typ.	Max.	Unit
VCC	Supply voltage	4.5	5.0	5.5	V
I	Supply current	500	560	600	mA
P_{max}	Max power consumption	2.25	2.80	3.30	W
RS422	Rx has onboard 120k Ω termination			3	Mbit/s
CAN	120 Ω termination - optional			1	Mbit/s
I^2C	200k pull-up to 3.3 V			400	kHz

Note: The NanoDock is powered with 5V and then it is powering the daughterboards, so you only need a single 5V supply for the NanoCom SDR.

7 RF Characteristics

The TR-600, which is basically a transceiver board, supports configurable bandwidth and carrier frequencies as outlined in the datasheet. The TR-600 is equipped with 2x TX/RX channels.

Description	Min.	Max.	Unit
TR-600 input level		5	dBm
Band	70 MHz	6000 MHz	MHz
Bandwidth	0.2 MHz	56 MHz	MHz

Note: The return loss and noise figure of the TR-600 will not determine the SDR system return loss and noise figure since the TR-600 always comes together with a front-end RF HW and an antenna like ANT-2000. The front-end will determine the system noise figure and not TR-600.

In other words, the front-end is responsible for optimizing RX noise figure, gain, TX output power, and provides proper filtering for the specific application. This means, that RX noise figure, TX output power, filtering etc. should be taken from the front-end and not from TR-600.

8 Physical Characteristics

8.1 Individual Components

NanoDock SDR

Description	Value	Unit
Mass	76.35	g
Size	Standard PC104 fit 90 x 66	mm

NanoMind Z7000 (with shield)

Description	Value	Unit
Mass	76.8	g
Size	65.0 x 40.0 x 6.5	mm

NanoCom TR-600 (with shield)

Description	Value	Unit
Mass	65.25	g
Size	65.0 x 40.0 x 14.8	mm

Slot shield

Description	Value	Unit
Mass	26.3	g

8.2 Complete System

NanoCom SDR (SDR Dock + Z7000 + TR-600 + two slot shields)

Description	Value	Unit
Mass	~ 271	g

NanoCom SDR (SDR Dock + Z7000 + two TR-600 + one slot shield)

Description	Value	Unit
Mass	~ 310	g

Note: There are slot shields placed in every empty slot.
Note: Numbers do not include rod, PIM, nuts, stack connector and foam.

9 Environment Testing

To simulate the harsh conditions of launch and space, the NanoDock SDR (SDR Dock, Z7000 and TR-600) has been exposed to a number of environment tests. For detailed information about the tests please contact GomSpace.

The NanoDock SDR has been in space and performed perfectly.

10 Physical Layout

A mounted daughterboard will have its shield thermal connected with the gold on the NanoDock SDR. The gold has a thermal connection to the gold on the other side of the PCB to even out the thermal load.

Small islands of electronics have been placed inside the gold to individual shield it. Notice there is only one daughterboard slot with an extra Samtec connector, to fit a NanoMind Z7000.

The physical layout of the daughterboards can be found in their respective datasheets.

10.1 Top

Stack connector on the right. Connectors on the left edge. Bottom left is the SD card slot. Through the middle are the connectors to the daughterboards (4x Samtec LSHM-150-04.0-L-DV-A-S-K-TR and 1x Samtec LSHM-130-04.0-L-DV-A-S-K-TR). The NanoMind Z7000 is placed in the bottom slot, whereas the slot at the top is used for the NanoCom TR-600.

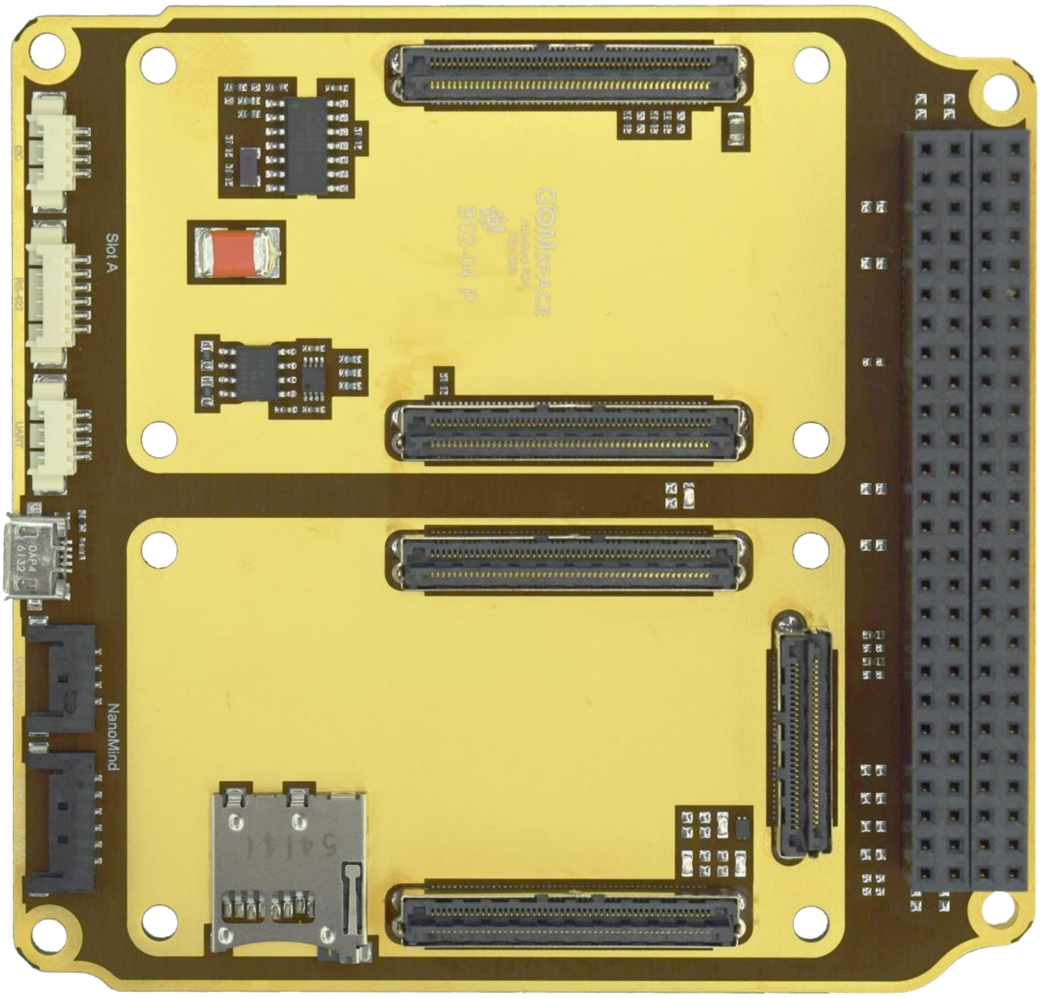


Fig. 10-1 NanoDock SDR (top)

In the top gold islands are the RTC and the RS422.

10.2 Bottom

Stack connector on the right. Connectors on the left side. Through the middle are the connectors to the daughterboards (4x Samtec LSHM-150-04.0-L-DV-A-S-K-TR). The two slots are for mounting two NanoCom TR-600s.

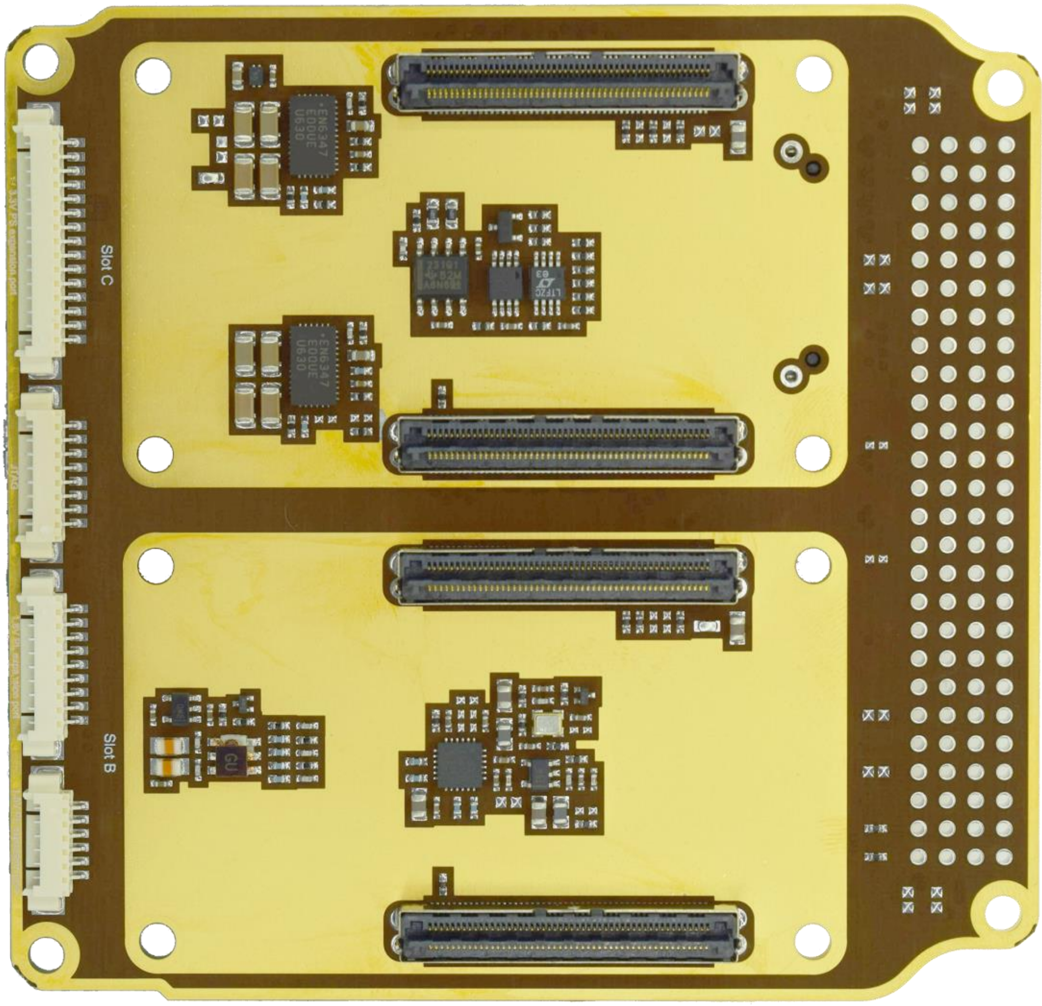


Fig. 10-2 NanoDock SDR (bottom)

In the top gold islands are the PSU (the two left most) and the CAN and I2C isolator in the middle. In the bottom island, mid is the clock fanout buffer.

11 Mechanical Drawing

All dimensions shown in the drawings below are in mm.

11.1 NanoDock SDR

A mechanical drawing of the NanoDock SDR is shown in Fig. 11-1.

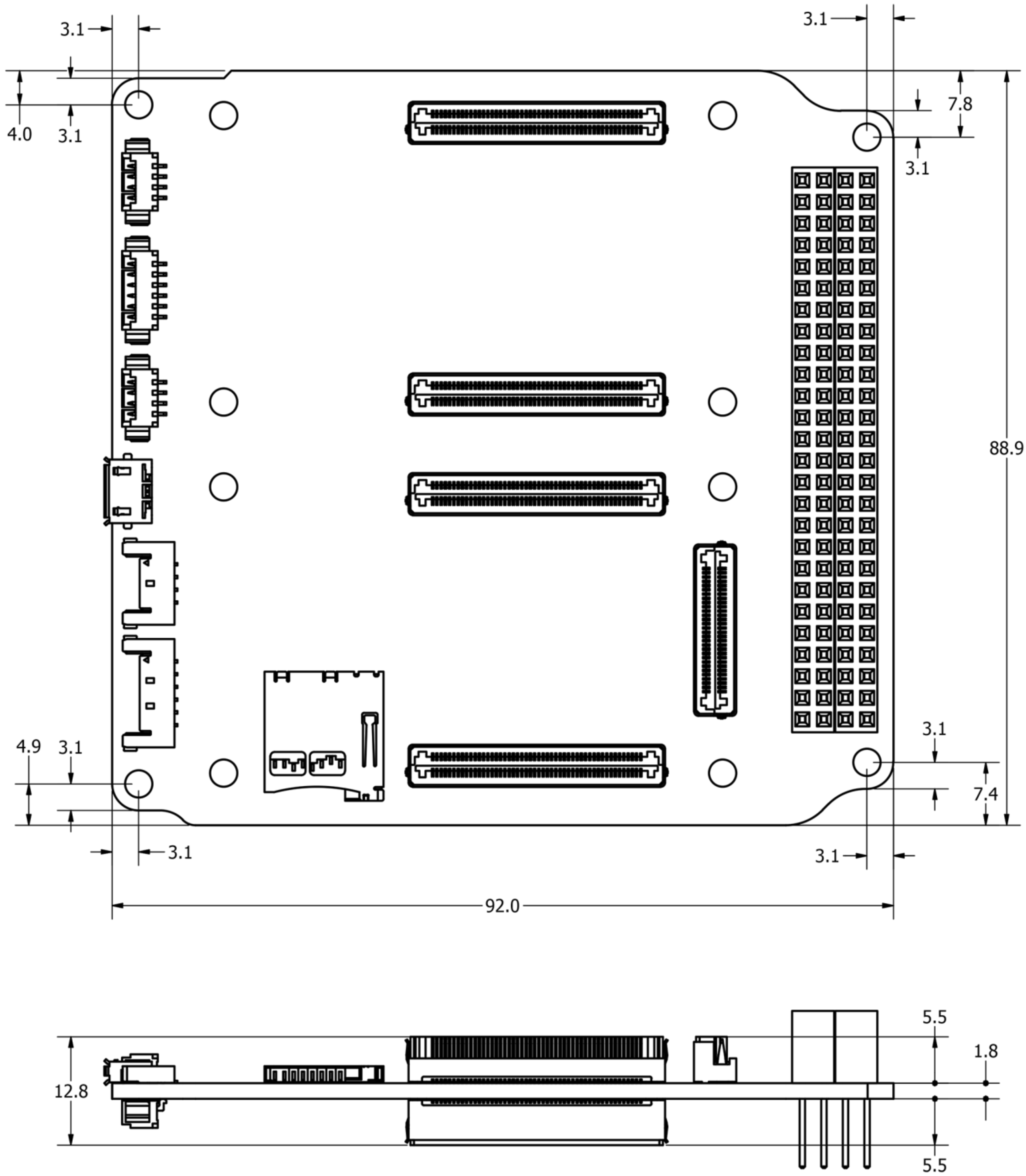


Fig. 11-1 Mechanical drawing of the NanoDock SDR

Fig. 11-2 shows a mechanical drawing of the NanoDock SDR with TR-600/Z7000 mounted. All dimensions are in mm.

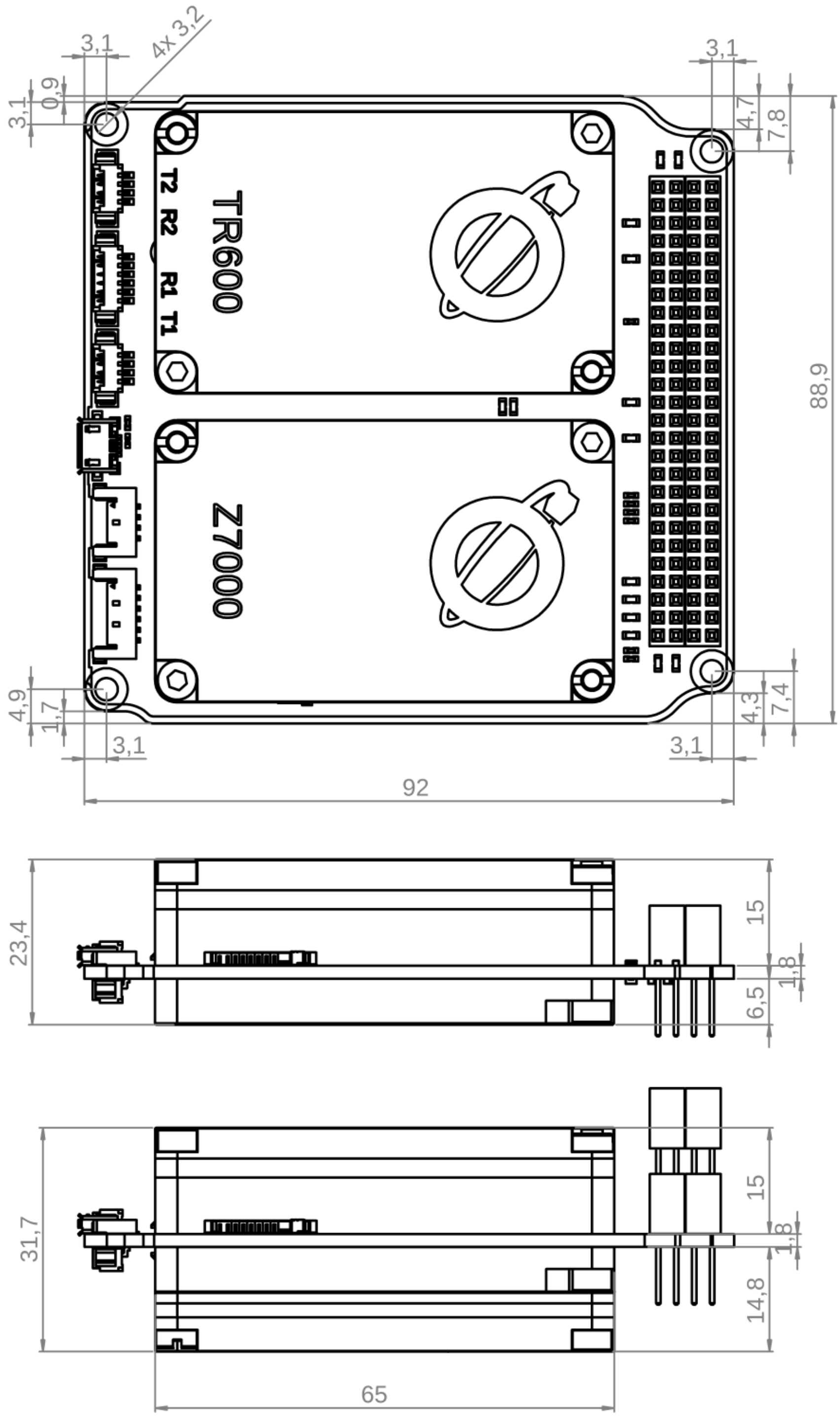


Fig. 11-2 Mechanical drawing of the NanoDock SDR with mounted daughterboards

11.2 NanoCom Z7000

See Fig. 11-3 for a mechanical drawing of Z7000.

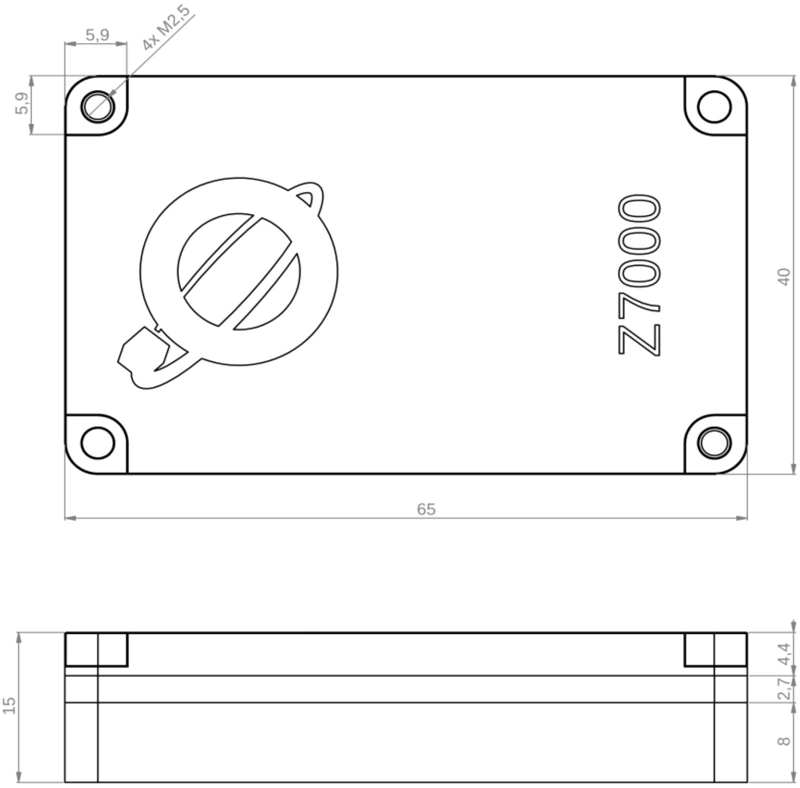


Fig. 11-3 Mechanical Drawing: Z7000

11.3 NanoCom TR-600

See Fig. 11-4 Mechanical Drawing: TR-600 for a mechanical drawing of TR-600.

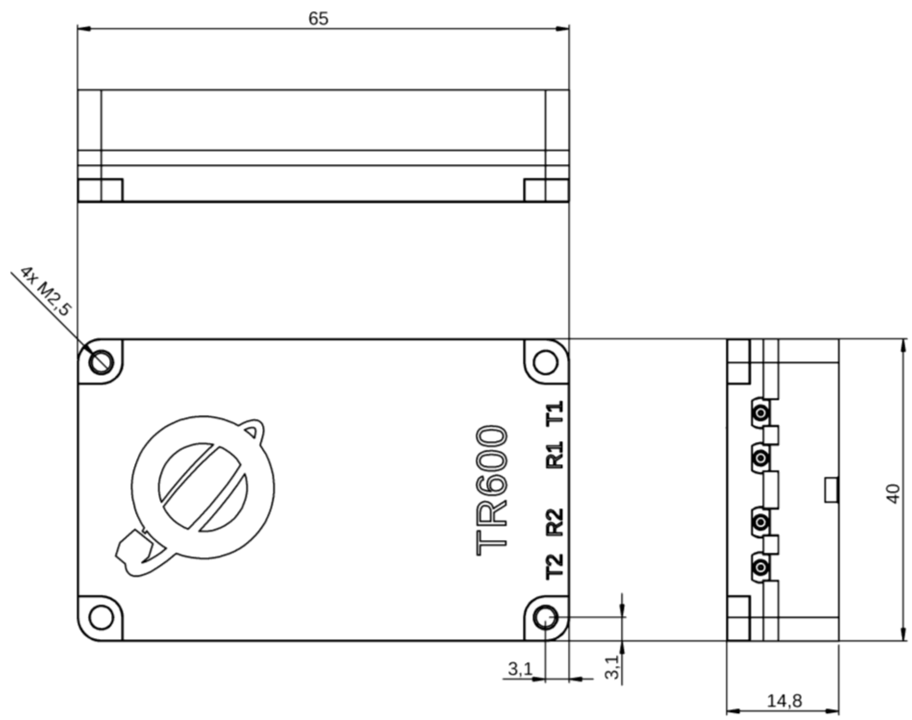


Fig. 11-4 Mechanical Drawing: TR-600

12 Disclaimer

The information in this document is subject to change without notice and should not be construed as a commitment by GomSpace. GomSpace assumes no responsibility for any errors that may appear in this document.

In no event shall GomSpace be liable for incidental or consequential damages arising from use of this document or the software and hardware described in this document.

13 Changelog