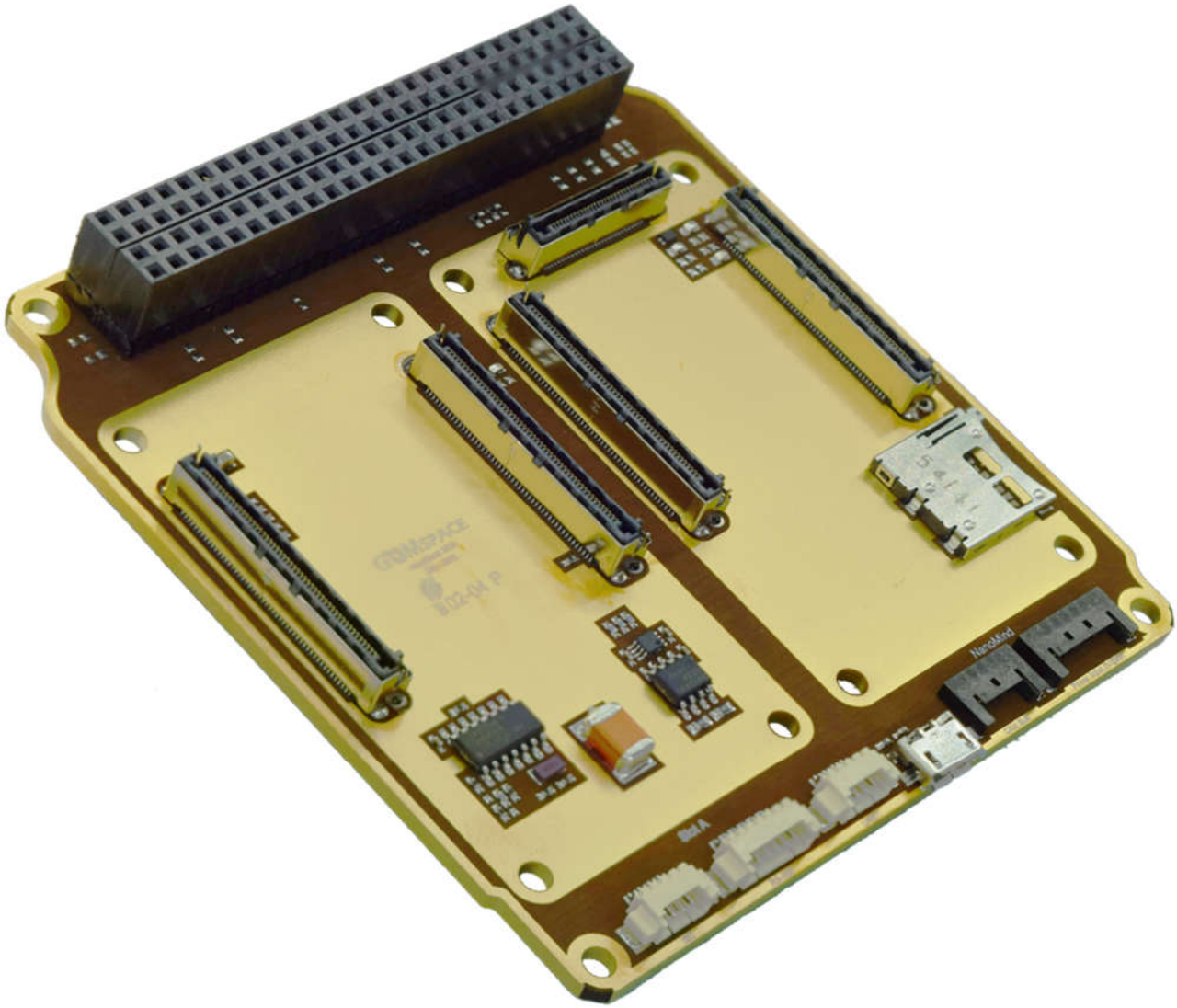

NanoDock
SDR

Datasheet

Carrier for 4 daughterboards for use in nano-satellites

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Product name: NanoDock SDR

Document No.: 1015263

Revision: 2.8

Author: KLK

Approved by: MJN

Approval date: April 2019

Confidentiality Notice

1 Table of Contents

2 Overview

The NanoDock SDR (here after SDR) together with a NanoMind Z7000 and NanoCom TR-600 is designed to be a modular CPU/FPGA and radio for small satellites. It is built around GomSpace modular technology, allowing numerous configurations of modules to be implemented on a motherboard, saving significant volume and giving customers a high level of customization.

Standard configuration includes:

- 1 NanoDock SDR motherboard
- 1 NanoMind Z7000 CPU daughterboard
- 1-3 NanoCom TR-600 radio daughterboard

2.1 Highlighted Features

NanoDock SDR motherboard

- GomSpace Motherboard – daughter board concept, up to 4 modules
- Centralized 40 MHz clock
- Fits standard PC104
- MicroSD card connector
- USB to UART console interface for easy use in lab setup
- Operational temperature: -20°C to +85°C
- Storage temperature: -20°C to +85°C
- Mass: 74.2 g
- PCB material: Glass/Polyimide IPC 6012C cl. 3/A
- IPC-A-610 Class 3 assembly

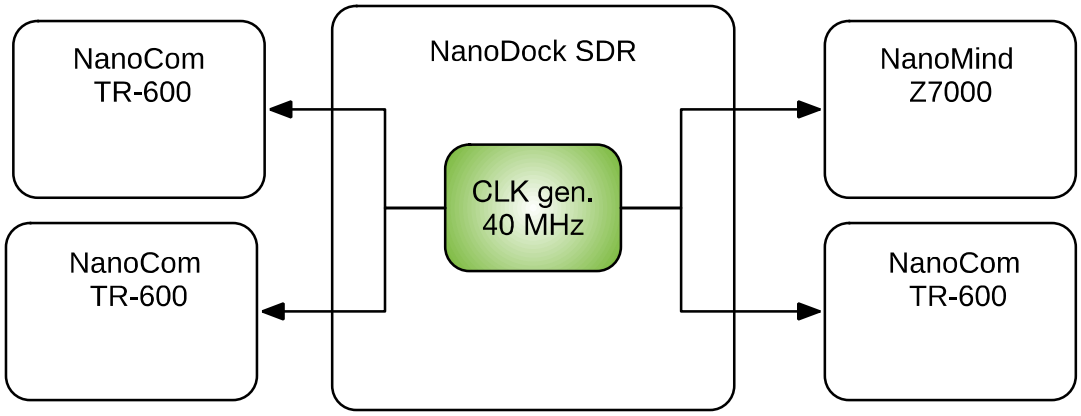
GomSpace SDR system solution

- Flight proven
- Integration with standard GomSpace EPS
- Precision milled anodized aluminum heat sinks to control thermal load and provide EMI shielding
- Fits in less than 0.3U volume in a nano-satellite / cubesat

2.2 Functional Description

2.2.1 Centralized Clock

The SDR has an integrated 40 MHz clock that can be used as a reference clock for the daughter boards. This is to prevent clock frequency drift between the different parts of the system.



2.2.2 Time Sync.

An external 1PPS can be taken from the stack and used for an external synchronization, eg a GPS sync signal. This is per default available, but can through option sheet choice be removed.

2.2.3 Programmable Logic (PL) 1.8 V

It is recommended to use IO pins supporting MRCC (Multi Region Clock Capable), if synchronization is needed in the FPGA. These pins are dedicated resources that reduce clock skew and jitter. If you are clocking something out, or reading something in with a reference clock, you want to put the clock on a MRCC pin.

A MRCC capable input/output is available on the stack connector pin H1_2 (3.3 V input) and on connector j19 pin 1 and 2 (1.8 V level). H1_2 can be used as a single-ended signal; J19 pin 1 and 2 can be use as differential or single-ended signal. When connecting a single-ended clock to the differential pair of pins, it must be connected to the positive (P) side of the pair.

2.2.4 Processing System (PS) 3.3 V

For best accuracy it is recommended to use pins supporting the dedicated TCC (Triple Timer Counters) instead of relying on the interrupt service routine along.

2.2.5 Synchronize to an external signal

Setup the TCC to trigger on the edge of the PPS signal and start counting. Now when needed you can read the width of the external pulse (measured in CPU-1X period) and calculate elapsed time from edge. By using the dedicated HW TCC you can eliminate any ISR delay.

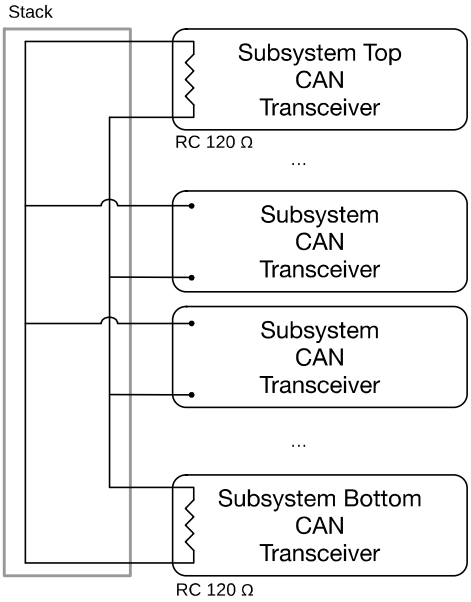
One TCC capable input is available on connector J12 pin 12 (MIO19).

2.2.6 I^2C Pull-up

The I^2C enable has 200k Ω pull-up resistor to 3.3 V.

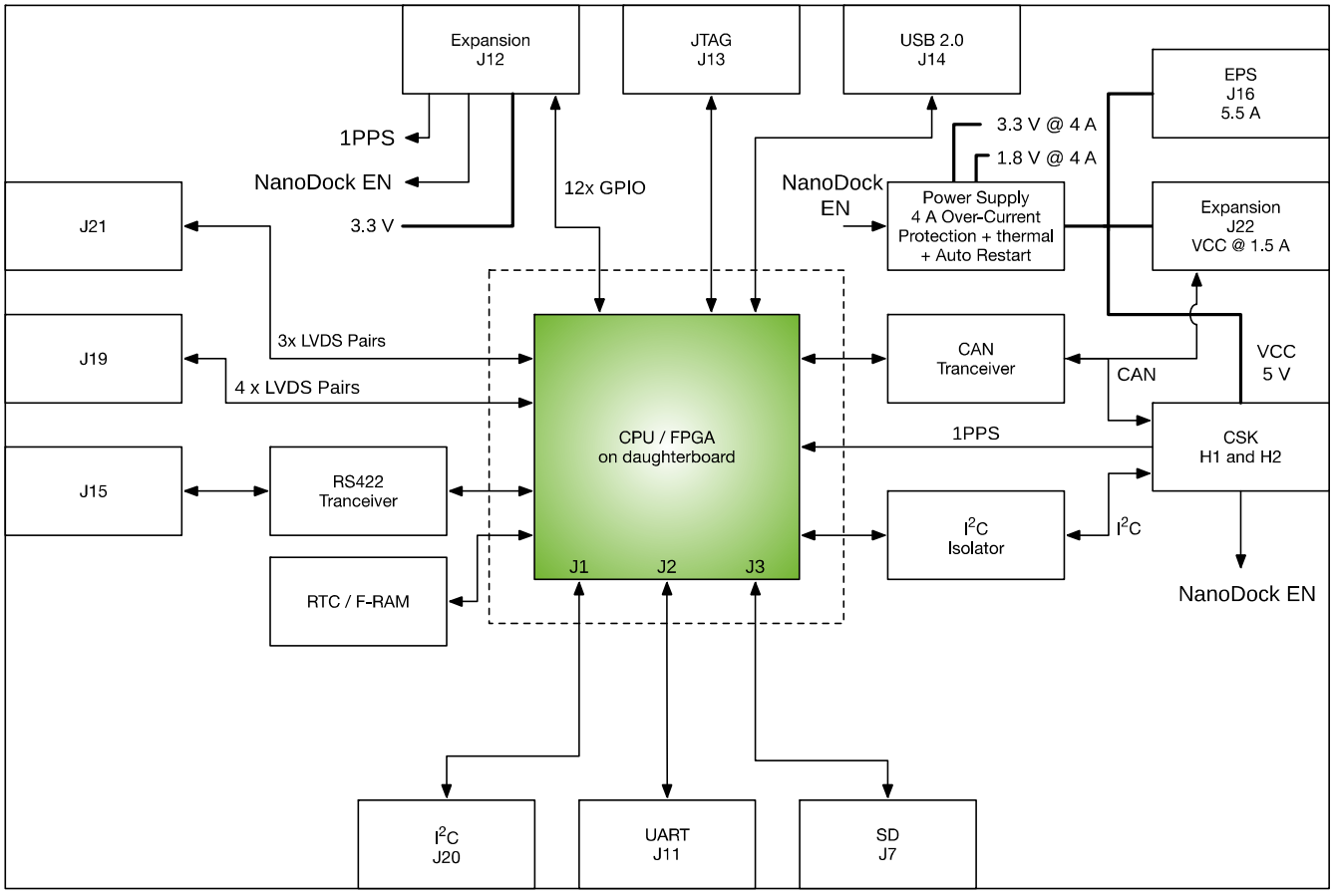
2.2.7 CAN Stack Termination Recommendation

GomSpace recommends having a 120 Ω termination resistor in the top and bottom of the CAN bus, to mitigate reflections. The total bus resistance should be 60 Ω. On the NanoDock SDR there is per default mounted a 120 Ω termination resistor, by option sheet choice it can be removed.

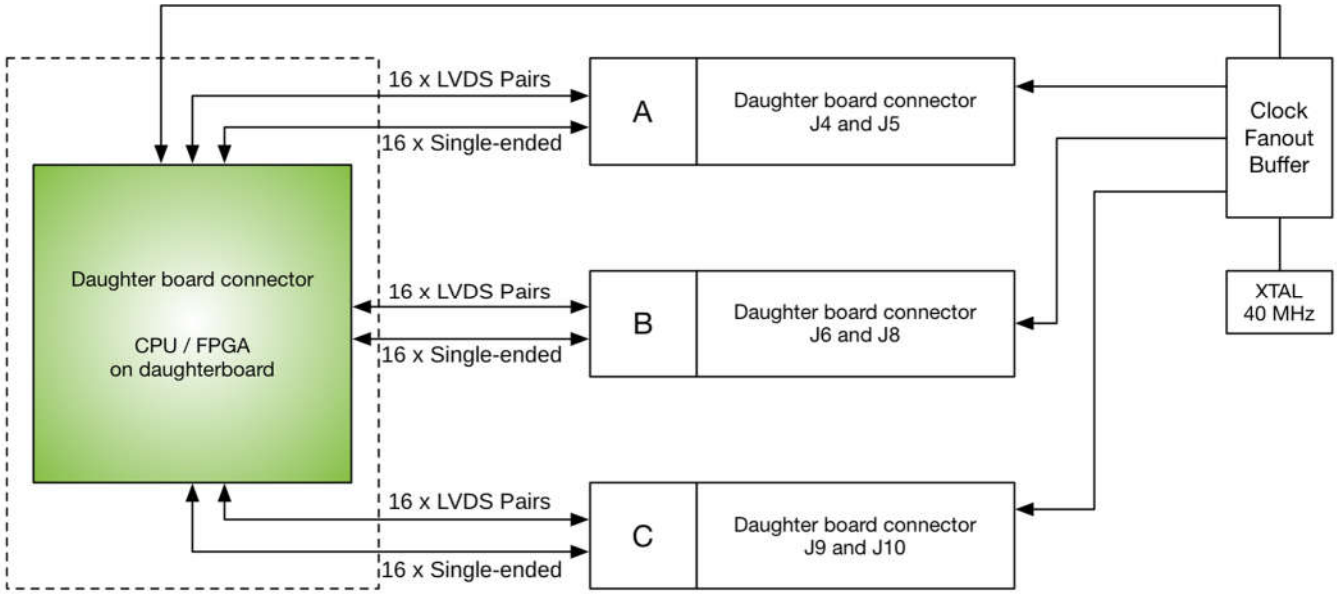


2.3 Block Diagram

2.3.1 CPU and Connectors

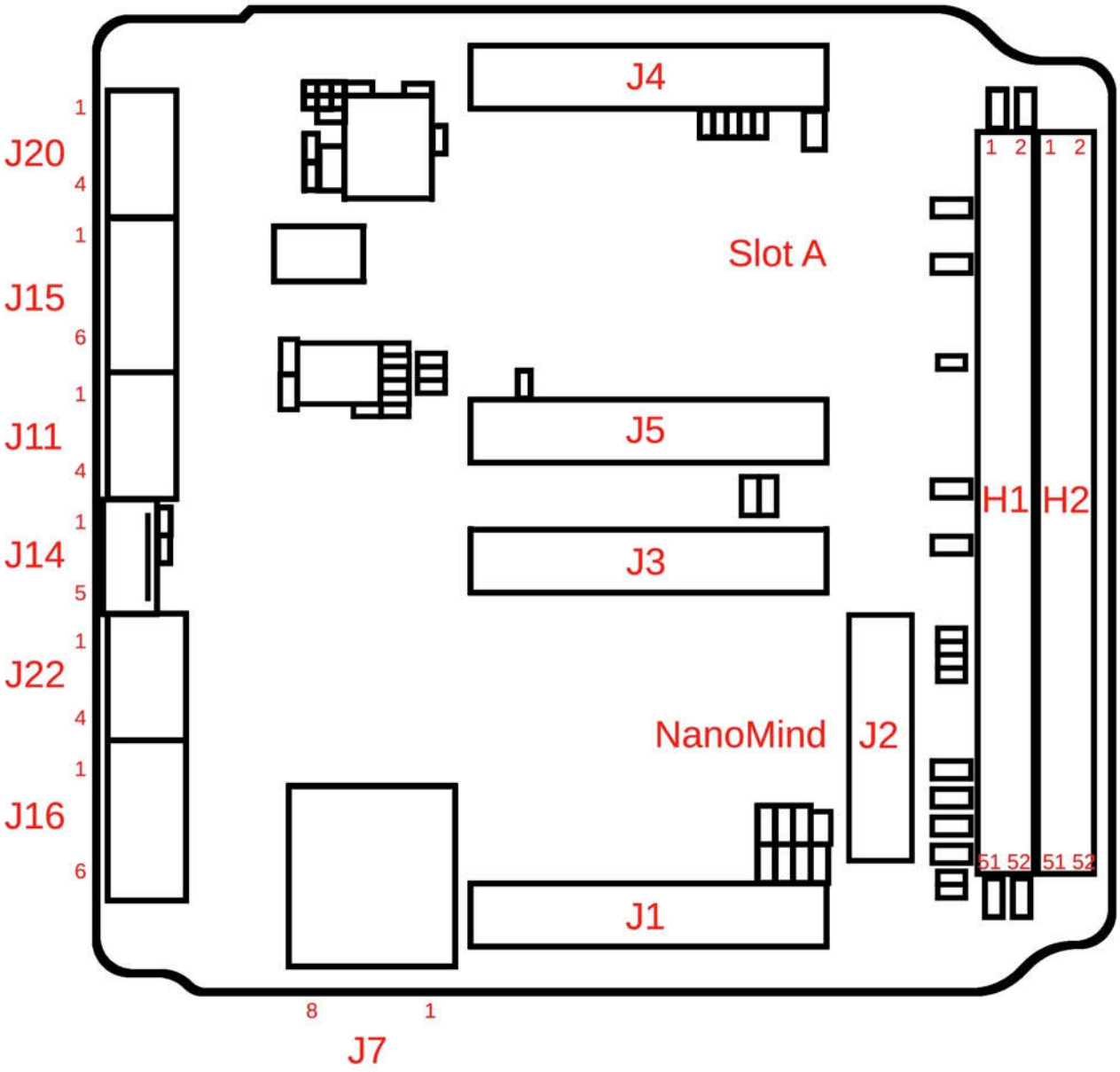


2.3.2 CPU Connection to Daughterboards



3 Connector Pinout

3.1 NanoDock SDR Top



3.1.1 H1/H2 - Stack Connector

H1

Pin	Description
1	CANL *
2	GPS heartbeat *
3	CANH *
41	CSK_SDA *
43	CSK_SCL *
45	GND *
46	GND *
47	VCC input option *
48	VCC input option *
49	VCC input option *
50	VCC input option *
51	VCC input option *
52	VCC input option *

H2

Pin	Description
1	VCC input option *
2	VCC input option *
3	VCC input option *
4	VCC input option *
5	VCC input option *
6	VCC input option *
7	GND *
8	GND *
27	VCC input option *
28	VCC input option *
29	GND
30	GND
32	GND
49	VCC input option *
51	VCC input option *

* Depending on option sheet choice

It is recommended to use connector J16 to power the NanoDock SDR. Powering through the stack can be used as secondary option. Depending on the distance from the EPS to the NanoDock SDR in the stack the voltage loss vary quite a bit. This can be mitigated by using more pins, so the current and voltage are within limits.

3.1.2 J7 – SD Card

Molex 500873-0806

Pin	Description
1	SDIO_0_IO2 *
2	SDIO_0_IO3 *
3	SDIO_0_CMD *
4	SD_VCC
5	SDIO_0_CLK *
6	GND
7	SDIO_0_IO0 *
8	SDIO_0_IO1 *

* The marked pins are mutually exclusive with marked pins on J12

3.1.3 J11 – 3.3 V UART

Molex PicoBlade 1.25 mm Pitch. 53261-0471.

Pin	Description
1	GND
2	n.c.
3	ARM_UART0_RX
4	ARM_UART0_TX

3.1.4 J14 - USB

Pin	Description
1	VBUS
2	USB_N
3	USB_P
4	OTG_ID
5	GND

3.1.5 J15 – RS422

Molex PicoBlade 1.25 mm Pitch. 53261-0671.

Pin	Description
1	TX_N
2	TX_P
3	GND
4	n.a.
5	RX_N with 120 Ω onboard termination
6	RX_P with 120 Ω onboard termination

3.1.6 J16 – EPS

Molex PicoLock 1.50 mm Pitch. 504050-0691.

Pin	Description
1	VCC
2	VCC
3	VCC
4	GND
5	GND
6	GND

3.1.7 J20- I²C

Molex PicoBlade 1.25 mm Pitch. 53261-0471.

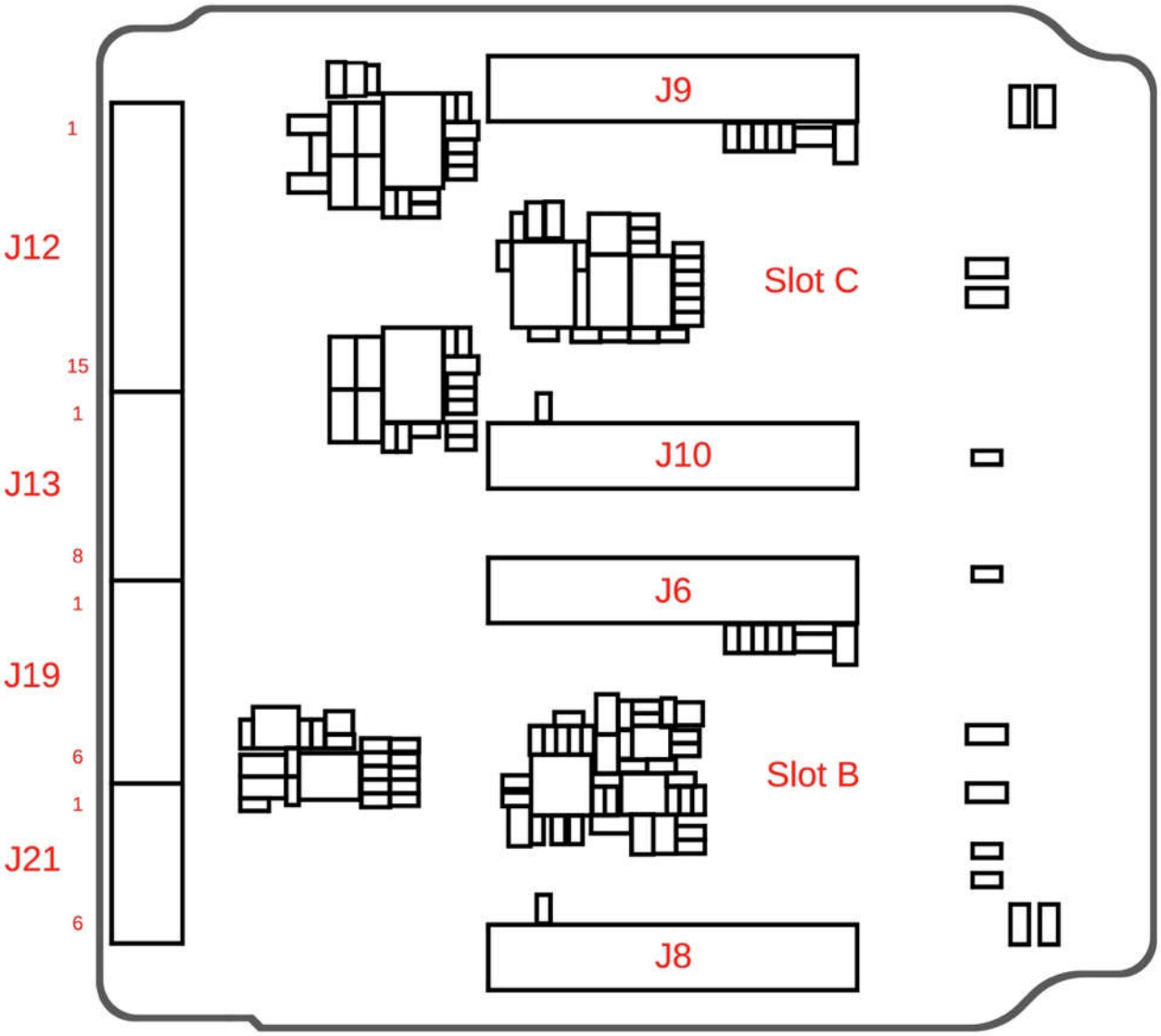
Pin	Description
1	ARM_SCL0 has 200k Ω pull-up resistor to 3.3 V.
2	ARM_SDA0 has 200k Ω pull-up resistor to 3.3 V.
3	3.3 V Supply Output
4	GND

3.1.8 J22 – Expansion

Molex PicoLock 1.50 mm Pitch. 504050-0491.

Pin	Description
1	GND
2	CANL
3	CANH
4	VCC

3.2 NanoDock SDR Bottom



3.2.1 J12 – 3.3 V Single-ended

Molex PicoBlade 1.25 mm Pitch. 53261-1571.

J12 and J7 (SD card) use the same signals so they each are mutually exclusive.

Pin	Description
1	PCA-P2
2	SDIO_0_CLK *
3	SDIO_0_IO0 *
4	SDIO_0_IO1 *
5	SDIO_0_CMD *
6	SDIO_0_IO3 *
7	SDIO_0_IO2 *
8	MIO23
9	CAN_Rs
10	MOI9
11	NanoDock EN has 143k Ω pull-up resistor to VCC **
12	MIO19
13	MOI0
14	3.3V_MB
15	GND

* The marked pins are mutually exclusive with marked pins on J7
** By pulling the signal low the NanoDock SDR and its daughterboards are turned off

3.2.2 J13 - JTAG

Molex PicoBlade 1.25 mm Pitch. 53261-0871.

Pin	Description
1	JTAG_TD0
2	JTAG_TCK
3	JTAG_TMS
4	JTAG_TDI
5	PB_SRST_B
6	PB_SRST_B
7	3.3 V Supply output
8	GND

3.2.3 J19 – 1.8 V LVDS/single-ended

Molex PicoBlade 1.25 mm Pitch. 53261-0971.

Pin	Description
1	L9_P_13
2	L9_N_13
3	L1_P_13
4	L1_N_13
5	GND
6	L20_N_33
7	L20_P_33
8	L22_N_33
9	L22_P_33

3.2.4 J21 – 1.8 V LVDS/single-ended

Molex PicoBlade 1.25 mm Pitch. 53261-0671.

Pin	Description
1	L18_N_13
2	L18_P_13
3	L23_N_13
4	L23_P_13
5	L24_N_13
6	L24_P_13

4 Absolute Maximum Ratings

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the NanoDock SDR. Exposure to absolute maximum rating conditions for extended periods may affect the reliability.

Symbol	Description	Min.	Max.	Unit
VCC	Supply voltage	4.0	6.5	V
I	Supply current	0.3	8.0	A
T_{amb}	Operating temperature	-20	85	°C
$T_{Storage}$	Storage temperature	-20	85	°C

5 Electrical Characteristics

For NanoDock SDR with one NanoMind Z7000 one NanoCom TR-600 and with standard software image idle.

Symbol	Description	Min.	Typ.	Max.	Unit
VCC	Supply voltage	4.5	5.0	5.5	V
I	Supply current	500	560	600	mA
P_{max}	Max power consumption	2.25	2.80	3.30	W
RS422	Rx has onboard 120k Ω termination			3	Mbit/s
CAN	120 Ω termination - optional			1	Mbit/s
I^2C	200k pull-up to 3.3 V			400	kHz

6 Physical Characteristics

Description	Value	Unit
Mass	76.4	g
Size	Standard PC104 fit 90 × 96	 mm

7 Environment Testing

To simulate the harsh conditions of launch and space, the NanoDock SDR has been exposed to a number of environment tests. For detailed information about the tests please contact GomSpace.

The NanoDock SDR has been in space and performed perfectly.

8 Physical Layout

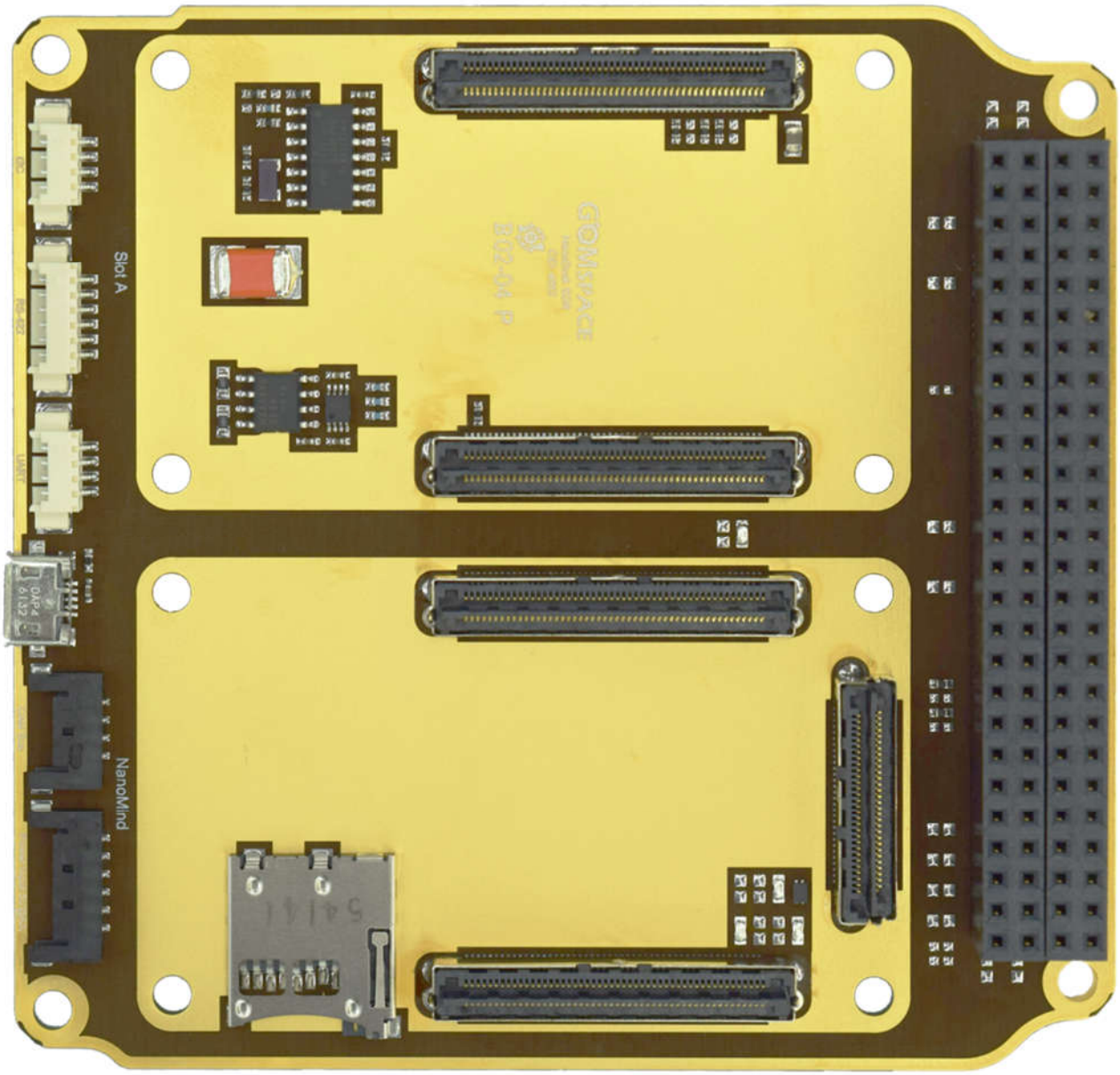
A mounted daughterboard will have its shield thermal connected with the gold on the NanoDock SDR. The gold have a thermal connection to the gold on the other side of the PCB to even out the thermal load.

Small islands of electronics has been placed inside the gold to individual shield it.

Notice there is only one daughterboard slot with an extra Samtec connector, to fit a NanoMind Z7000.

8.1 Top

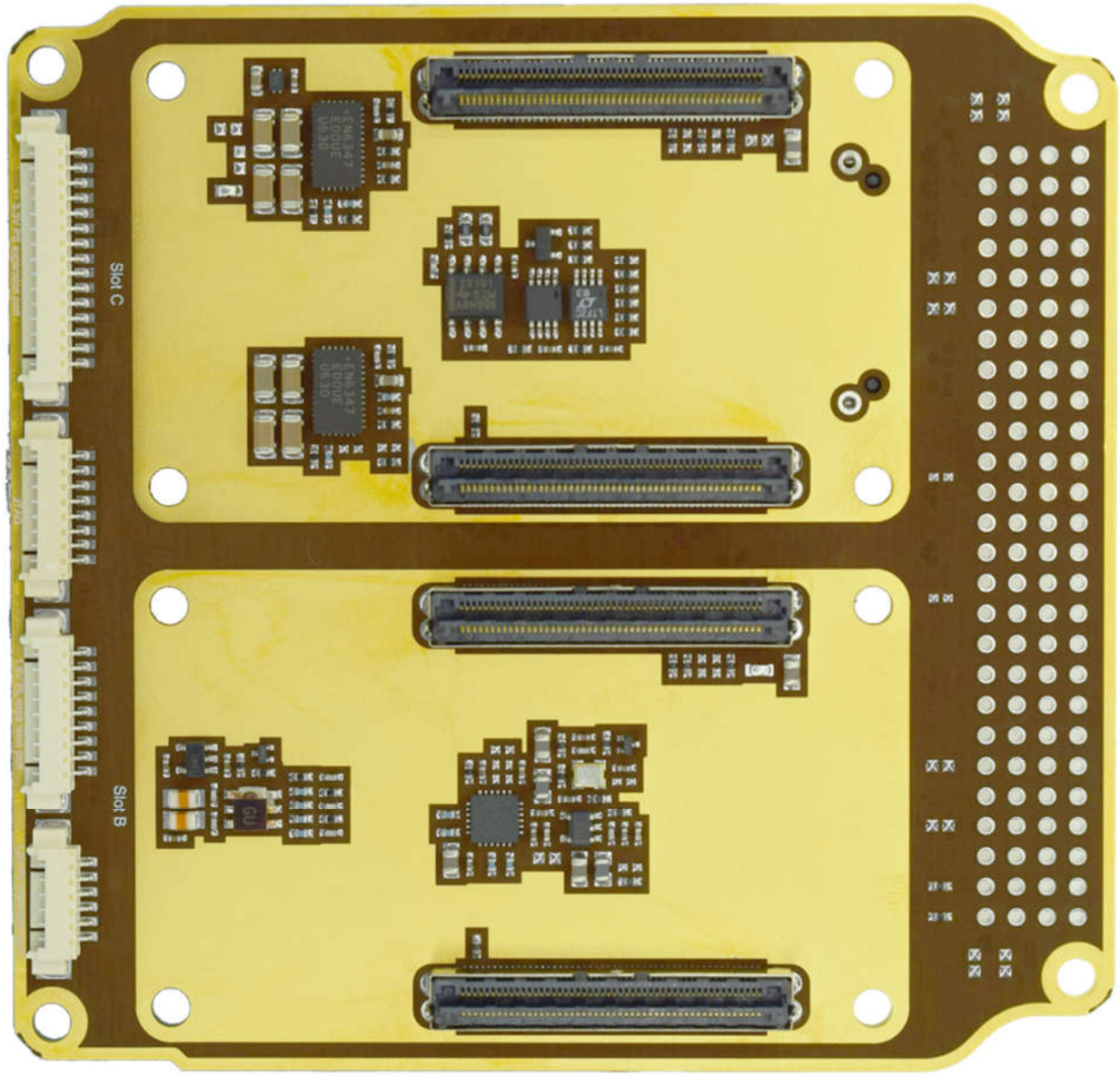
Stack connector on the right. Connectors on the left edge. Bottom left is the SD card slot. Through the middle are the connectors to the daughterboards (4x Samtec LSHM-150-04.0-L-DV-A-S-K-TR and 1x Samtec LSHM-130-04.0-L-DV-A-S-K-TR).



In the top gold islands are the RTC and the RS422.

8.2 Bottom

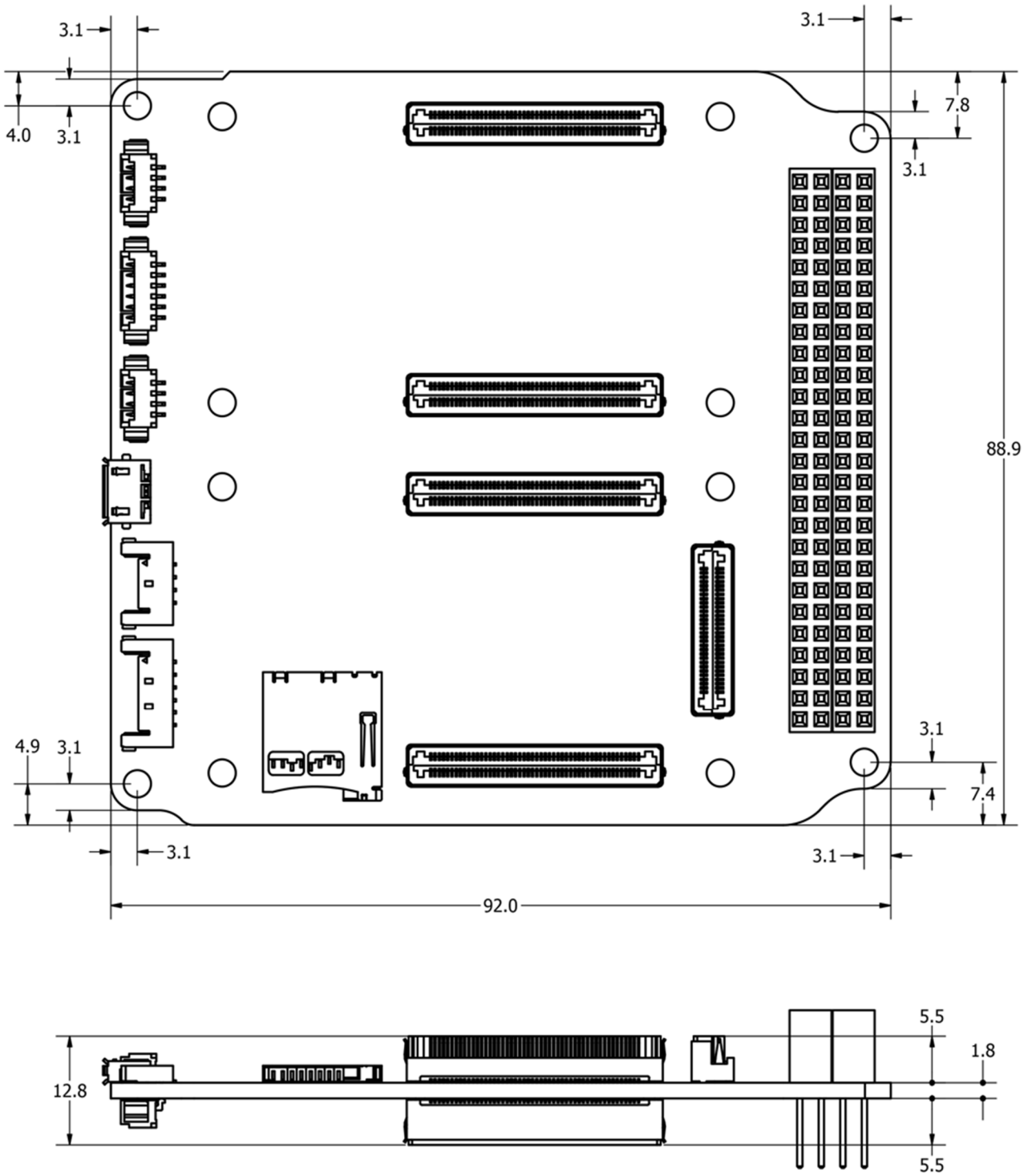
Stack connector on the right. Connectors on the left side. Through the middle are the connectors to the daughterboards (4x Samtec LSHM-150-04.0-L-DV-A-S-K-TR).).



In the top gold islands are the PSU (the two left most) and the CAN and I^2C isolator in the middle. In the bottom island mid is the clock fanout buffer.

9 Mechanical Drawing

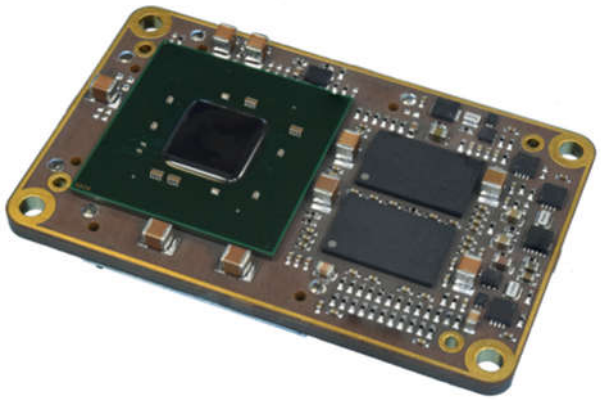
All dimensions in mm.



10 Related Products

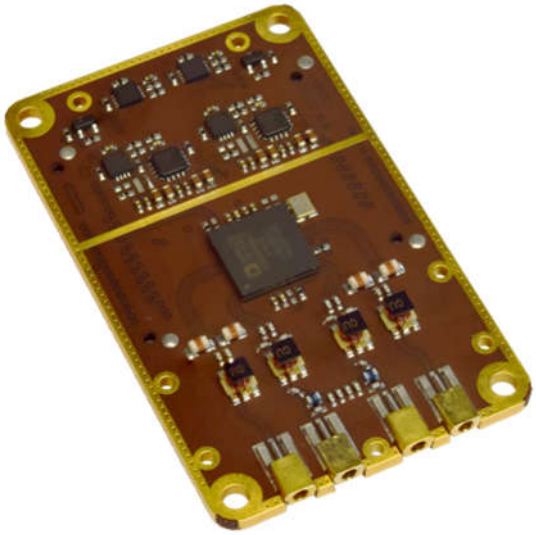
10.1 NanoMind Z7000

Is a powerful processer module that can be mounted on top of the NanoDock SDR. The module contains two parts: a ARM/FPGA and a divided power system. Only one can be mounted at a time. The system is encased in an aluminum shield.



10.2 NanoCom TR-600

A radio module with four antenna connectors. Up to three of these can be mounted on the NanoDock SDR. The system is encased in an aluminum shield.



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