# NanoMind

# A712D

# Datasheet

On-board Computer System for mission critical space
application with limited resources

# 1 Table of contents

## 2  Changelog

| Date | Revision | Author | Description |
|---|---|---|---|
| 11/12-2013 | 1.0 | KK | First draft |
| 15/5-2014 | 1.1 | KK | Update text. New layout |
| 12/11-2014 | 1.2 | KK | Update |
| 5/6-2015 | 1.3 | KK | Update |
| 4/8-2015 | 1.4 | KK | Update |
| 1/9-2015 | 1.5 | JDC/KLK | Updated text. New layout |
| 18/3-2016 | 1.6 | KLK | Added magnetometer picture in chap. 3.5 |

# 3   Overview

The NanoMind A712D (A712D) on-board computer is designed as an efficient system for space applications with limited resources, such as e.g. for Cubesat or nano-satellite missions. In addition to a fully capable computer system it provides a 3-Axis magnetometer to sense the Earth's magnetic field and coil-drivers that can be used to implement attitude control based on magnetic sensing and actuation. Its main interface to other subsystems are a CAN bus and an $I^2C$ bus.

## 3.1   Feature Overview

- High-performance 32-bit ARM7 RISC CPU
- Compatible with FreeRTOS and eCos realtime operating systems
- Extensive software library for FreeRTOS
- Clock speed: 8-40 MHz
- 2 MB Static RAM
- 4 MB Data Storage (Flash Memory)
- 4 MB Code Storage (Flash Memory)
- 2 GB MicroSD card support
- 104-pin CubeSatKit bus connector
- CAN bus interface
- $I^2C$ interface (two separate busses available)
- USART interfaces
- RTC - real time clock w/backup power keeps time 30-60 minutes without external power
- On-board temperature sensors
- GPIO pins
- Attitude stabilization system:
  - 3-Axis magneto resistive sensor
  - 3 PWM bidirectional output 3.3-5 V/±3 A
  - Interface to 6-analog inputs (e.g. sun sensors)
  - SPI interface to e.g. gyroscopes
- Power monitor/ power-on reset.
- 3.3 V single supply voltage.
- Temperature tolerance -40 to 85 °C.
- PCB: Space grade Glass/Polyamide IPC 6012C cl. 3/A
- Dimensions: 96 mm x 90 mm x 10 mm. Fits standard PC104
- Mass: 50-55 g (depending on configuration)

## 3.2   Microcontroller

The computer is based on the ARM7TDMI embedded processor. This processor has a high-performance 32-bit RISC architecture with a high-density 16-bit instruction set and very low power consumption.

## 3.3   CAN Bus Interface

One of the main interfaces of the A712D to communicate with other subsystem hardware is a CAN bus interface. The Controller Area Network (CAN) is a serial communications protocol that supports distributed real-time control with a high level of security. The maximum bus speed is 1 Mbits/s.

The A712D uses the SN65HVD230 as a CAN transceiver. Designed for operation in harsh environments, this device features cross-wire protection, loss-of-ground and over-voltage protection, over-temperature protection, as well as wide common mode range. This device provides different modes of operation: high-speed, slope control, and low-power modes.

## 3.4   I²C Interface

The A712D has an I²C bus supporting bidirectional data transfer between masters and slaves, multi-master bus, arbitration between simultaneously transmitting masters without corruption of serial data on the bus. Serial clock synchronization allows devices with different bit rates to communicate via one serial bus and is used as a handshake mechanism to suspend and resume serial transfer.

The I²C bus provides a high-speed of 400 kbit/s, with a transmit hardware buffer of 68 bytes and a receive hardware buffer of 68 bytes (packets can be longer than buffer size).

## 3.5   3-Axis Magnetometer

The A712D includes a 3-Axis magnetometer to sense the Earth's magnetic field, the HMC5843 from Honeywell. The device is based in the Honeywell's Anisotropic Magnetoresistive (AMR) technology. The sensor features precision in-axis sensitivity and linearity, and its solid-state construction with very low cross-axis sensitivity designed to measure both direction and magnitude of Earth's magnetic field, from 10 micro-gauss to 4 gauss.

The magnetometer directions are shown in the drawing below, showing the top of the A712D PCB.
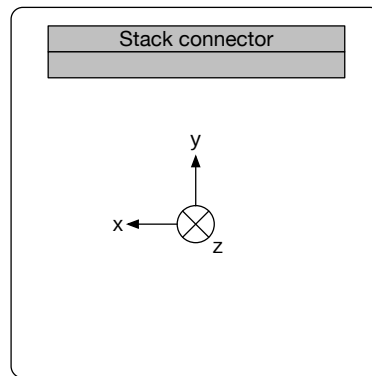


The magnetometer interfaces to the MCU via a dedicated I²C bus using a software driver included in the software library.

## 3.6   3-PWM Bidirectional Output

The A712D has 3 bidirectional outputs from 3 H-bridge drivers designed to be controlled by a PWM output from the microcontroller. The main purpose of these bidirectional outputs is to be used for external magnetorquers to implement attitude control. The drivers are fully compatible with the GomSpace NanoPower solar panel products.

## 3.7   Analog Input

The A712D provides an analog interface to connect six photodiodes to measure the incident sunlight. The interface is fully compatible to the GomSpace NanoPower solar panel products.

## 3.8   GPIO

General-purpose digital logic inputs/outputs on the microcontroller are made available in the stack connector. These all operate on 3.3 V CMOS logic levels and can be accessed through the software API.

## 3.9   Software

The system is prepared for operation with the FreeRTOS realtime operating system and a software framework is included to allow a swift start-up of the on-board software development. The software

package includes an Eclipse based development library, library with device drivers, and a tool for debugging & software upload.

## 3.10 Block Diagram

A block diagram of the system and its interfaces is provided on the figure below:
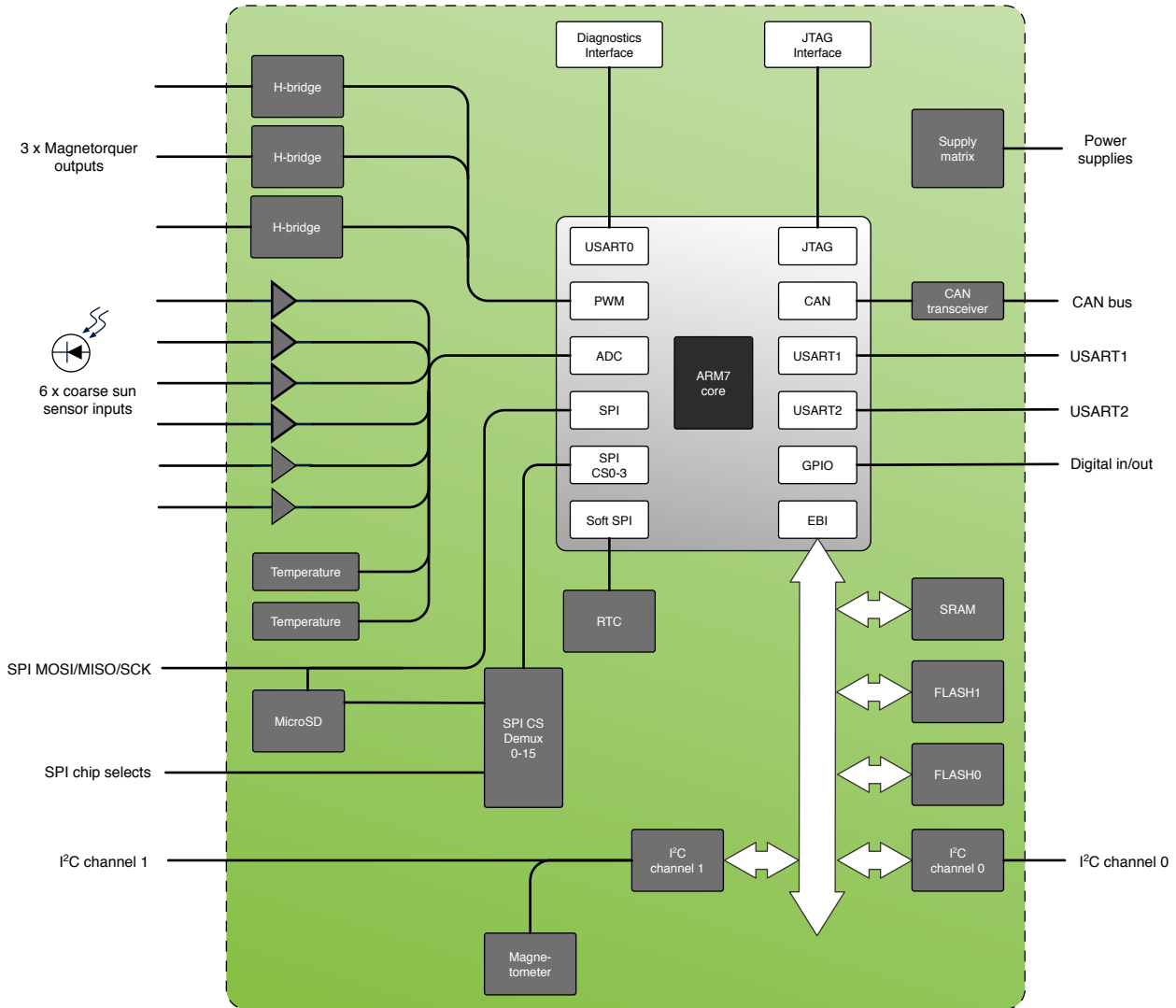
# 4  Hardware Layout

## 4.1  Connector Location Top

The NanoMind A712D is equipped with the following connectors:

**H1+H2**: 104 pin CubeSatKit connector (SAMTEC ESQ-126-49-G-D or compatible)

**A1-A6**: Signals for external photo-diodes, gyros, temp.sensor and magnetorquers. The interface is fully compatible with the GomSpace NanoPower Solar Panel products

**WE**: Jumper to protect the code storage flash memory

**Diag**: Diagnostics input module

**USART**: extra USART interface

**I²C**: Access to the I²C interface used by the magnetometer

**JTAG**: Programming and debugging interface

The drawing below shows the connection on the top of the circuit board.

## 4.2  Stack Connector H1/H2

The following table shows the pinout for the CubeSat Kit Connector H1 and H2. Some pins are shown multiple times as they can be configured to either of multiple options.

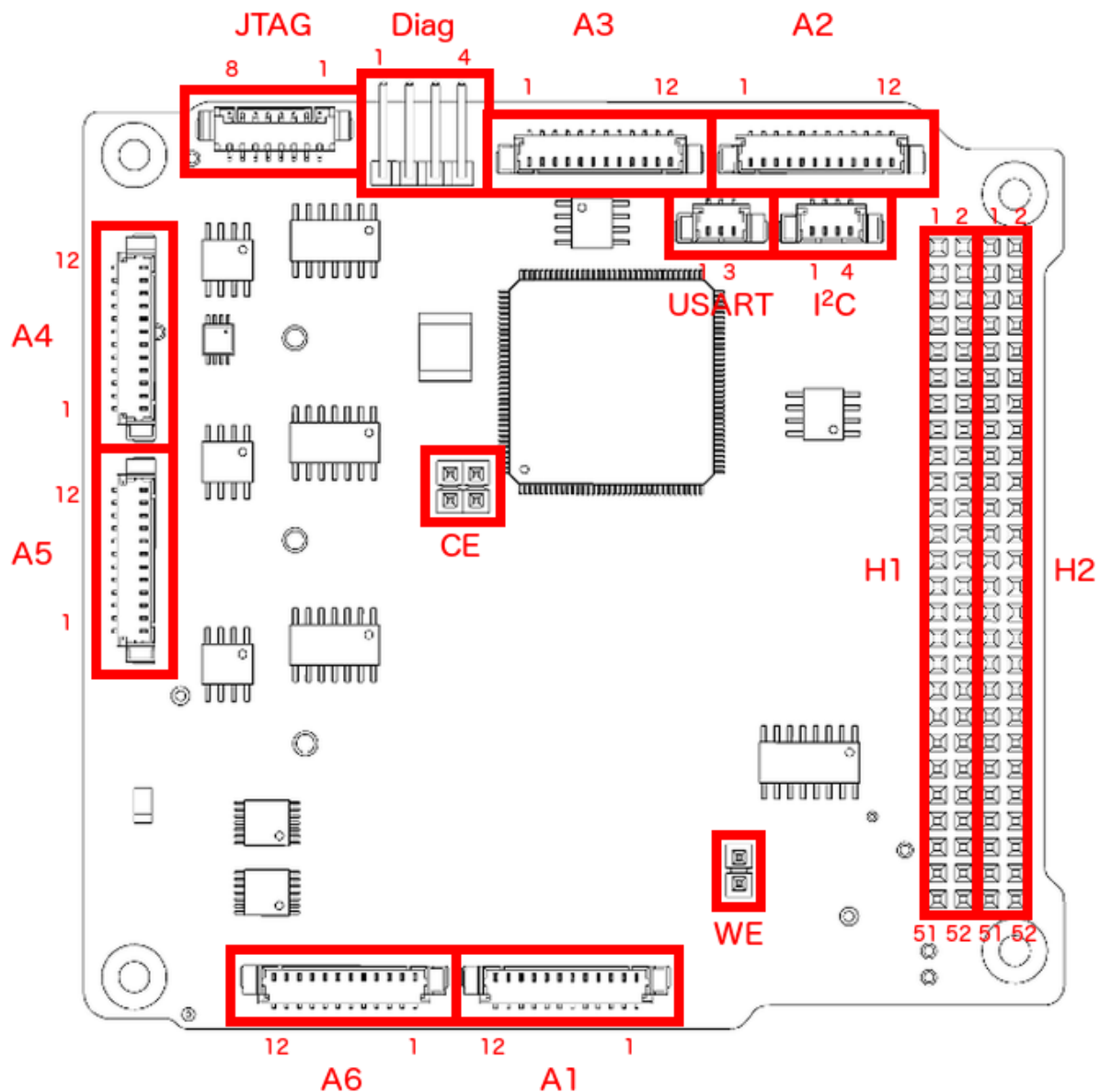|       | Pin     | Electrical specifications           | A712D                 |
|-------|---------|-------------------------------------|-----------------------|
| **H1** | 1 (A)   | CAN bus, 3.3V, 120R, diff. low      | CANL (Bi)             |
|       | 1 (B)   | 3.3 V LVCMOS                        | GPIO CPU pin 51 (Bi)  |
| **H1** | 2       | 3.3 V LVCMOS                        | GPIO CPU pin 53 (Bi)  |
| **H1** | 3       | CAN bus, 3.3 V, 120R, diff. high    | CANH (Bi)             |
| **H1** | 9       | 3.3 V LVCMOS open-drain             | SPI CS1 (output)      |
| **H1** | 10      | 3.3 V LVCMOS open-drain             | SPI CS2 (output)      |
| **H1** | 11      | 3.3 V LVCMOS open-drain             | SPI CS3 (output)      |
| **H1** | 12      | 3.3 V LVCMOS open-drain             | SPI CS4 (output)      |
| **H1** | 13      | 3.3 V LVCMOS open-drain             | SPI CS5 (output)      |
| **H1** | 14      | 3.3 V LVCMOS open-drain             | SPI CS6 (output)      |
| **H1** | 18      | 3.3 V LVCMOS                        | GPIO CPU pin 48 (Bi)  |
| **H1** | 19      | UART, 3.3 V, 500kbaud               | UART2 RX (input)      |
| **H1** | 20      | UART, 3.3 V, 500kbaud               | UART2 TX (output)     |
| **H1** | 21      | 3.3 V LVCMOS                        | SPI CLK (output)      |
| **H1** | 22      | 3.3 V LVCMOS                        | SPI MISO (input)      |
| **H1** | 23      | 3.3 V LVCMOS                        | SPI MOSI (output)     |
| **H1** | 24      | 3.3 V LVCMOS open-drain             | SPI CS7 (output)      |
| **H1** | 26      | 3.3 V LVCMOS                        | GPIO CPU pin 47 (Bi)  |
| **H1** | 29      | 3.3 V LVCMOS                        | GPIO CPU pin 52 (Bi)  |
| **H1** | 33      | UART, 3.3 V, 500 kbaud              | UART1 RX (input)      |
| **H1** | 35      | UART, 3.3 V, 500 kbaud              | UART1 TX (output)     |
| **H1** | 41      | $I^2$C SDA, LVCMOS (3.3 V)          | Bi (100k pull-up)     |
| **H1** | 43      | $I^2$C SCL, LVCMOS (3.3 V)          | Bi (100k pull-up)     |
| **H1** | 45      | $I^2$C SDA2, LVCMOS (3.3 V)         | Bi (100k pull-up)     |
| **H1** | 47 (A)  | 3.3 V, 2 A                          | VCC input option      |
|       | 47 (B)  | $I^2$C SCL2, LVCMOS (3.3 V)         | Bi (100k pull-up)     |
| **H1** | 48      | 3.3 V, 2 A                          | VCC input option      |
| **H1** | 49 (A)  | 5 V, 2 A                            | VCC input option      |
|       | 49 (B)  | 3.3 V LVCMOS                        | GPIO CPU pin 50 (Bi)  |
| **H1** | 50      | 3.3 V, 2 A                          | VCC input option      |
| **H1** | 51      | 5 V, 2 A                            | VCC input option      |
| **H1** | 52      | 3.3 V, 2 A                          | VCC input option      |
| **H2** | 27      | 3.3 V, 5 A                          | VCC input option      |
| **H2** | 28      | 3.3 V, 5 A                          | VCC input option      |
| **H2** | 29      | Power ground                        | GND                   |
| **H2** | 30      | Power ground                        | GND                   |
| **H2** | 50      | 3.3 V LVCMOS                        | GPIO CPU pin 49 (Bi)  |

## 4.3 Picoblade A1 – A6

| Pin | Description |
|-----|-------------|
| 1 | PWM B (only available in connector A4, A5 & A6) |
| 2 | PWM A (only available in connector A4, A5 & A6) |
| 3 | GND |
| 4 | Vgyro (option sheet dependent) |
| 5 | SPI chip select 1 (active low) |
| 6 | SPI MOSI |
| 7 | AGND (analogue ground, reference pin 5) |
| 8 | Photo-diode analog input |
| 9 | SPI SCLK |
| 10 | SPI MISO |
| 11 | VCC (option sheet dependent) |
| 12 | SPI chip select 2 (active low) |

## 4.4 Diag

| Pin | Description |
|-----|-------------|
| 1 | GND (black wire on Diag interface!! Left-most pin on drawing on previous page) |
| 2 | VCC 3.3 V supply input (*Do not use this when powered from the stack connector*) |
| 3 | RX (USART0 input 3.3 V 8N1 500 kbps) |
| 4 | TX (USART0 output 3.3 V 8N1 500 kbps) |

## 4.5 USART Picoblade

| Pin | Description |
|-----|-------------|
| 1 | RX (USART2 input 3.3 V 8N1 500 kbps) |
| 2 | TX (USART2 output 3.3 V 8N1 500 kbps) |
| 3 | GND |

## 4.6 I²C Picoblade

| Pin | Description |
|-----|-------------|
| 1 | SCL |
| 2 | SDA |
| 3 | VCC |
| 4 | GND |

## 4.7 WE

Apply jumper to enable writing on FLASH0

## 4.8 CS (EBI memory)

Default position routes chip select 0 to FLASH0 and chip select 1 to FLASH1. If needed, the jumpers can be rotated 90 degrees to route chip select 0 to FLASH1 and chip select 1 to FLASH0.

## 4.9 SPI Channel

The A712D has two SPI chip-selects on each side panel. When using the GomSpace NanoPower Solar P100U side panels, the SPI chip select on pin 5 is used for a Gyro and the chip select on pin 12 for an LM70 temperature sensor. Furthermore, an SPI channel is used for the SD-Card interface. The following table lists the chip select allocations for the different panel connectors and the optional memory.

| Connector | PIN 12 | PIN 5 |
|-----------|--------|-------|
| A1 | CS2 | CS1 |
| A2 | CS4 | CS3 |
| A3 | CS6 | CS5 |
| A4 | CS9 | CS8 |
| A5 | CS11 | CS10 |
| A6 | CS13 | CS12 |
| SD-Card | CS7 | |

# 5  General Characteristics

| Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| VCC | Supply voltage | 3.08 | 3.30 | 3.40 | V |
| Reset Voltage | | | 3.06 | | V |
| Current Consumption, 3.3V | Executing from RAM:<br>  40 MHz nominal<br>  8 MHz<br>Additional current consumption:<br>  Erasing FLASH<br>  Writing to FLASH<br>  Executing from FLASH (e.g. at startup)<br>  Magnetometer on<br>  CAN bus | | 70.0<br>37.0<br><br>8.9<br>5.1<br>3.0<br>5.3<br>10.0 | 89.0<br>48.0<br><br>11.0<br>6.0<br><br><br>17.0 | mA |
| Clock Frequency | | 8 | 40 | 40 | MHz |
| Operating temperature | | -40 | | 60 | °C |
| PWM output<br>- Supply voltage<br>- Voltage output<br>- Current output<br>- Frequency<br>- Resolution | Maximum per channel AND total for all | 3.3<br>-5 | <br><br><br>153<br>8 | 5<br>5<br>3<br>1M | V<br>V<br>A<br>Hz<br>bit |
| Photo-diode input<br>- Input current<br><br>- Resolution | Current resulting in saturated measurement<br>Analog to digital conversion | | <br><br>10 | 1.67 | mA<br>bit |
| Magnetometer<br>- Field range<br>- Measurement time<br>- Resolution<br>- SNR | | -4 | <br>10<br>7<br>70 | 4 | gauss<br>ms<br>mG<br>dB |
| I²C<br>- Voltage<br>- Bit-rate | | 0 | 337 | 3.3<br>400 | V<br>kbps |

# 6  GomSpace Shell (GOSH) Interface

The A712D computer is equipped with a diagnostics interface enabling interaction with the computer via a simple console-like debugging screen. The interface consists of a logic-level RS232 connectio. The USB connection is capable of powering the A712D so no external power supply is needed to start testing and uploading software. The interface runs at "500000 baud 8N1" RS232 emulation via USB using a FTDI device driver so using a terminal program connected to the virtual COM port the following start-up screen should appear a few seconds after connecting the diagnostics interface to the A712D computer.

```
GomSpace built-in shell (gosh)
Enter 'help' for a list of built-in commands.

#
```

**Connecting the Diagnostics Interface**

The pinout of the diagnostics connector is shown on a previous page. Make sure that the black (ground) wire is connected to GND. Then insert the USB cable. The diagnostics interface supplies 3.3 V to the board so no other supply is needed and no other supply should be connected at the same time. The supply wire on the diagnostics interface is red and can be removed if it is desired to supply the board via another supply source.

*Warning: Do not try to supply the board from both the diagnostics interface and another supply at the same time!*

# 7 Software

GomSpace has developed an extensive set of libraries for the GomSpace NanoMind A712D computer, all this software comes as standard, except for the file system source-code.

## 7.1 Compiler: (arm-none-eabi)

GomSpace provides a custom ARM compiler for the A712D computer, which includes the newlib c-library. In general any arm-none-eabi compiler can be used, but all GomSpace code is compiled and tested using our specific build. So in order to avoid issues related to different compilers, it is recommended to use the provided compiler.

## 7.2 Board support package: (liba712)

The board support package contains code to boot and bring up the board to a working state using the FreeRTOS operation system. Furthermore, a set of peripheral drivers which includes I$^2$C, SPI, USART, ADC, Flash memory, Magnetometer, PWM (magnetorquer) and AIC interrupt controller.

## 7.3 CSP Network Stack: (libcsp)

The CSP network stack is a basis for communication between GomSpace products. This is lightweight network stack for cubesats. libcsp is opensource and can be found on libcsp.org.

## 7.4 File Transfer Protocol: (libftp)

For software uploads and data download, a full FTP implementation is provided. This uses RDP (a part of libcsp) for reliable communication, flow-control and automatic retransmissions. Libftp also supports pausing and resuming of file transfers. The FTP server has support for RAM, FAT and UFFS filesystem.

## 7.5 GomSpace Shell: (libgosh)

GOSH is an interactive console interface available for many of GomSpace products. It is mainly used for commanding subsystems through an extensive client library. GOSH is also available for ground station use (on a linux PC) and commands can then be sent to the A712D computer using CSP.

## 7.6 Logging system: (liblog)

The logging system takes care of many hundreds sources for debug information. It is categorized into logging groups, generally one group per driver or code module, and into logging levels such as, error, warning, info, debug and trace.

## 7.7 Parameter system: (libparam)

The universal parameter system is used by several of GomSpace latest products. The A712D itself does not use it, but since several of the latest GomSpace products uses this library, it is provided as a client.

## 7.8 Utility functions: (libutil)

Several extra small functions such as, clock management, file compression (lzo), byte-reordering, vmem (virtual-memory) interface and a convenient hex_dump function resides in this library.

## 7.9 File system: (libstorage)

The storage library contains a version of Chan's FAT FS ported for the A712D and with driver support for the SD-Card. For the on-board NOR flash, the UFFS filesystem is also provided. Both of these filesystems integrate with newlib's POSIX interface using a virtual filesystem layer called VFS.

# 8 Memory Layout

The general memory layout is shown in the figure below.
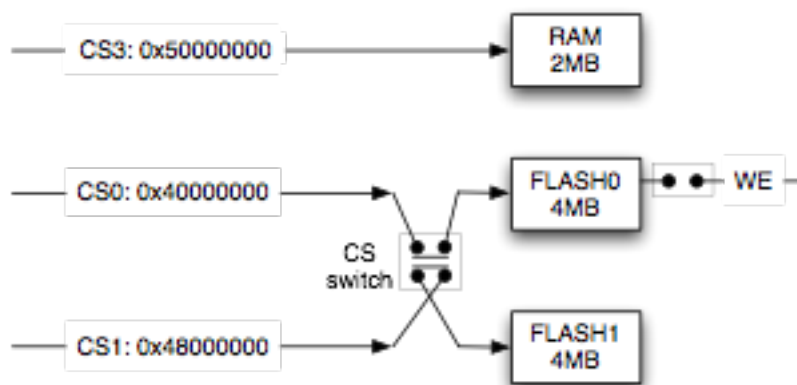


RAM is connected to chip select 3, which is mapped to address 0x50000000 spanning 2 MB. FLASH1 (User/Data storage) is default connected to CS1 mapped to address 0x48000000. FLASH0 (Read-Only, ROM) is default connected to CS0 mapped to address 0x40000000.

Both FLASH chips are the Atmel AT49BV320DT, and internal block layout can be obtained from the datasheet from Atmel.

The CS switch allows swapping the connection of chips select 0 and 1 making it possible to boot from FLASH1 in case something unintended has happened to the bootstrap in FLASH0.

*Note: These chip-select numbers are for the EBI interface, and should not be confused with the SPI chip-select numbers.*

## 8.1 Boot sequence

When the system is powered up and the reset signal is de-asserted by the reset controller, the computer starts execution from address 0x0 which is mapped to 0x40000000 on CS0, which means the instruction on address 0x0 in FLASH0 is the first instruction to be fetched.

After a system reset, the ROM image sets up the memory controller, and stack pointer. It then calls the c-function `low_level_init()` in boot.c. This function initializes the PLL to increase the speed of the processor from 8 MHz to 40 MHz and sets up the AIC (Advanced Interrupt Controller), it also copies the .data section from ROM to RAM and clears the .bss section. After calling *low_level_init()* the *main()* function is called using a long jump.

When the main-routine starts, it initializes the UART and the CSP network stack. This ensures communication is possible at an early stage of the boot process. Then it starts several tasks that are default in the ROM image.

Console Task: Enables commanding the NanoMind A712D OBC using the serial port.
Server Task: Enables the CSP protocol using serial port or I$^2$C.
USART RX Task: Helper task for the DMA USART driver, needed to be able to run 500.000 baud
Init Task: Initializes filesystem, mounts devices and runs the boot sequence shown below.

After starting the tasks, the scheduler will enter the idle state if no processing is required from any of the tasks. The idle task will make the CPU sleep in order to save power.

## 8.2 Loading an image to RAM

During the boot sequence, the init task will check the filesystem and search for a boot configuration file. If this exists it will look for the specified image-file and copy it to ram and check the checksum. If all goes well the image is executed from RAM, if at any point an error occurs during this process the default ROM image continues to execute. Before executing a loaded software image, the boot configuration is deleted. This is a safety measure to ensure the system will not enter an endless reboot-loop if the software image is invalid.

In order to have the same image startup again, the image must itself restore the boot configuration file using the *obc_boot_conf()* function. **Caution:** It is important not to call this function before every part of the software is verified and all necessary tasks are up and running so it is absolutely certain that the boot-up sequence does not cause a crash as this will put the system into an endless reboot-loop which cannot be detected by the boot-loader.
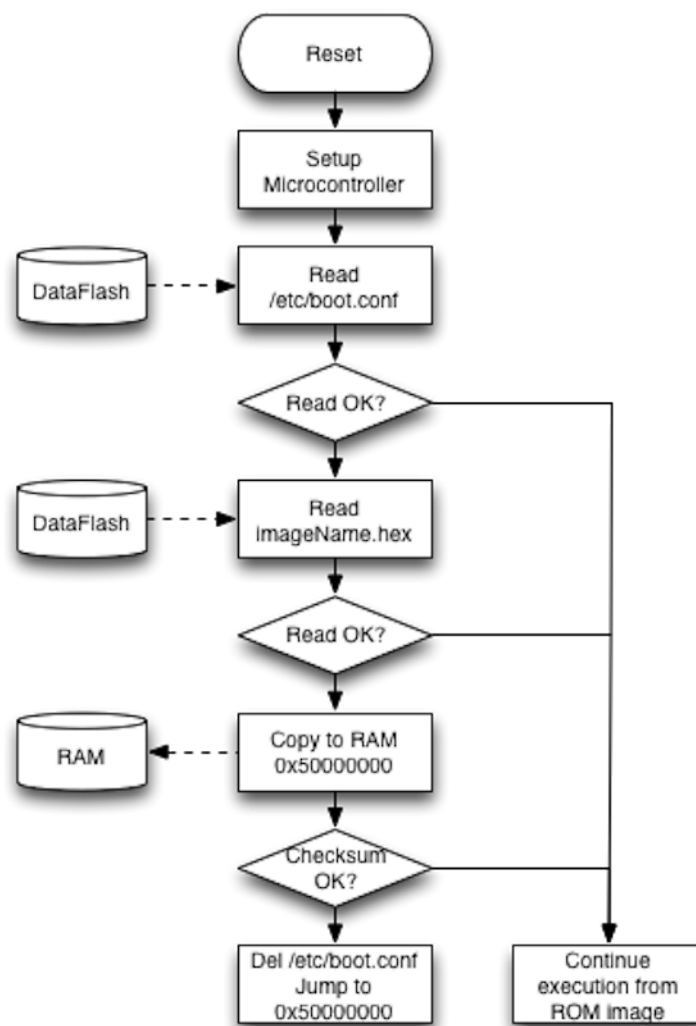
# 9 Operations and Handling

The NanoMind A712D system employs components based on CMOS and therefore requires anti-static handling precautions to be observed. Do not touch or handle the product without proper grounding!

# 10 Customization Options

As GomSpace realizes that different applications place different requirements to a computer system, the A712D products present a variety of options for customization. Options to be agreed upon time of order placement include:
• All pin-connections indicated with red dots
• Different conversion factors for analogue measurements may be implemented
• Conformal coating using NASA approved CV-1152 silicone coating (at an extra cost)
• More options may be available at the customers request

# 11 Quality Assembly

GomSpace space hardware is hand-assembled in a procedure where all parts are cleaned with IPA and then soldered in an anti-static environment to "IPC-A-610 Class 3" specifications. All solder-work is done under a microscope with tin-lead 63/37 using rosin flux. All solder joints are re-checked for class 3 compliance and the PCB is finally cleaned with IPA and ready for testing.

# 12 Physical Dimensions

Dimensions are given in mm.