NanoCom SDR MK3

Datasheet

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Product name: NanoCom SDR MK3

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Confidentiality Notice

List of abbreviations

Acronyms	Definitions
ADC	Analog to Digital Converter
AFE	Antenna Front-End
AGC	Automatic Gain Control
AI	Artificial Intelligence
BSP	Board Support Package
CAN	Controller Area Network
CLK	Clock
CSP	CubeSat Space Protocol
CTRL	Control
DAC	Digital to Analog Converter
dB	Decibel
dBc	Decibel relative to the carrier
DDR	Double Data Rate
DS	Datasheet
DUT	Design Under Test
eMMC	embedded MultiMediaCard
ENR	Excess Noise Ratio
EVM	Error Vector Magnitude
FIR	Finite Impulse Response
FPGA	Field-Programmable Gate Array
FTDI	Future Technology Devices International Limited
GB	GigaByte
GND	Ground
HDL	Hardware Description Language
HLOS	High Level Operating System
HW	Hardware
I/O or IO	Input/Output
I2C	Inter-Integrated Circuit
IOPS	Input/output Operations Per Second
IP	Intellectual Property
IQ	Quadrature signals
JTAG	Joint Test Action Group
LDO	Low Dropout
LNA	Low Noise Amplifier
LO	Local Oscillator
LVCMOS	Low Voltage Complementary Metal Oxide Semiconductor
LVDS	Low-Voltage Differential Signaling
MB	MegaByte
MIO	Multiplexed Input/Output
ML	Machine Learning
MLC	Multi Level Cell
MTU	Maximum Transmission Unit
MCS	Multi-Chip Synchronization
NC	Not Connected
NF	Noise Figure
PCB	Printed Circuit Board
PDK	Platform Development Kit
PL	Programmable Logic
PPS	Pulse Per Second
PS	Processing System
pSLC	pseudo Single Level Cell
PSU	Power Supply
PWR	Power
RAM	Random-Access Memory
RF	Radio frequency
RMS	Root Mean Square
RSSI	Received Signal Strength Indication
RX	Receiver
SCL	Serial Clock
SDA	Serial Data
SDK	Software Development Kit
SDR	Software Defined Radio
SE	Single Ended
SIGNIT	Signals Intelligence
SMPM	Sub-Miniature Push-on Micro
SoC	System on Chip
SPW	SpaceWire
SW	Software
TCK	Test Clock
TCP	Transmission Control Protocol
TDI	Test Data In
TDO	Test Data Out
TMS	Test Mode Select
TTL	Transistor-Transistor Logic
TX	Transmitter
UART	Universal Asynchronous Receiver Transmitter
UDP	User Datagram Protocol
USB	Universal Serial Bus
VCTCXO	Voltage Controlled Temperature Compensated Crystal Oscillator
YP	Yocto Project

Table of Contents

1 Overview

Figure 1.1: NanoCom SDR MK3

1.1 Highlighted Features

- Xilinx Zynq 7030/7045 Programmable SoC
  - Dual ARM Cortex A9 MPCore, up to 800MHz
  - Powerful FPGA with 125k/350k logic cells
- 1GB DDR3 RAM
  - 512MB with Error Correction Code enabled
- 256MB NOR flash
- 70GB eMMC (pSLC) and 233GB eMMC (MLC)
  - HW Bit-Flip Detection
  - Redundant Firmware Image
  - Option for Logical Volume Management (striping, mirroring, etc.)
- High speed interfaces
  - SpaceWire
  - USB (host/device)
- Up to three TR600 (based on AD9361)
  - 70 MHz to 6 GHz
  - Channel BW tuneable 200 kHz to 56 MHz
  - Support TDD and FDD operation.
- SMPM RF connectors
- AFE control interfaces
  - I2C, CAN, AuxDAC, AuxADC, +4.6V
- Flight heritage

1.2 Description

GomSpace's flight proven NanoCom SDR MK3 is a uniquely modular and compact high performance SDR platform, built to support custom RF applications. Featuring a powerful Zynq®7030/45 System on a Chip (SoC) at its core, its small form factor can incorporate up to three NanoCom TR600 MK3 Transceivers, each offering 2xRX and 2xTX Channels, making it a truly flexible, versatile, and cost-effective solution.

This flexibility allows a very wide range of custom applications. Whether high data rate intensive applications such as SIGINT/Spectrum Monitoring, or custom broadband and multiband communications, or even narrowband IoT and tracking solutions, NanoCom SDR MK3 can be configured for the mission.

With hardware prepared for Store and Forward, NanoCom SDR MK3 is also a perfect choice for custom intersatellite link / crosslink solutions for constellations or Non Terrestrial Network data relay applications.

NanoCom SDR MK3 comes with a wealth of configurable I/O and is complemented by GomSpace's wide portfolio of antenna solutions, to aid quick, efficient and flexible integration. For rapid development of custom SDR applications, GomSpace provides a comprehensive platform development kit as well as an optional, in depth, SDR standard training course which includes time for customer specific topics.

The platform development kit provides reference designs for both normal SDR operation as well as multi-chip synchronization operation. The normal operation enables independent transmit and receive operation on up to three NanoCom TR600 MK3 transceivers.

Multi-chip synchronization operation is tailored for signal intelligence, hereunder monitoring applications where synchronous sampling of a common RF signal is needed from 4 to 6 different RX paths on multiple NanoCom TR600 MK3 transceivers. Multi-chip synchronization is for reception only and ensures that the individual ADCs

used to sample RX signals are synchronized across TR600 slots. By using an external test signal, e.g. accessible via one of the TX ports on TR600 in slot B, it is furthermore possible to correct up to +/-180deg residual RX phase difference between individual receive paths.

2 Absolute Maximum Ratings

Parameter	Connectors	Min Value	Max Value	Unit
Supply Voltage (Main/Backup) V_{in}	J19, J20	-0.3	36	V
SpaceWire / LVDS voltage levels	J7, J8, J9, J10	-0.4	2.6	V
CAN voltage levels	J5, J6, J15, J16, J17	-60	60	V
RS422/RS485 voltage levels	J5, J6, J11, J13, J14	0	4	V
CLK voltage levels	J5, J6	-0.3	2.0	V
I2C voltage levels	J5, J6	-0.3	7.0	V
PPS voltage levels	J5, J6	-0.5	4.0	V
IO voltage levels	J4, J12, J18	-0.3	3.6	V
USB voltage levels	J2	-0.3	6	V
RF inputs (Peak Power)	RX-RF SMPM		+5	dBm
Thermal interface temperature		-40	50	°C
Storage Temperature		-40	85	°C

Table 2.1: Absolute maximum ratings

*Ratings given in this table are the absolute maximum values the device can handle under stress or transient conditions. The device should **not** be operated under these conditions. Exceeding these values may cause permanent damage to the NanoCom SDR MK3 assembly and/or externally connected devices. Please refer to section 8 for recommended operating conditions.*

3 Block Diagram

A high-level block diagram of the product is provided in Figure 3.1 and the detailed TR600 block diagram (same for Slot A, B and C) in Figure 3.2

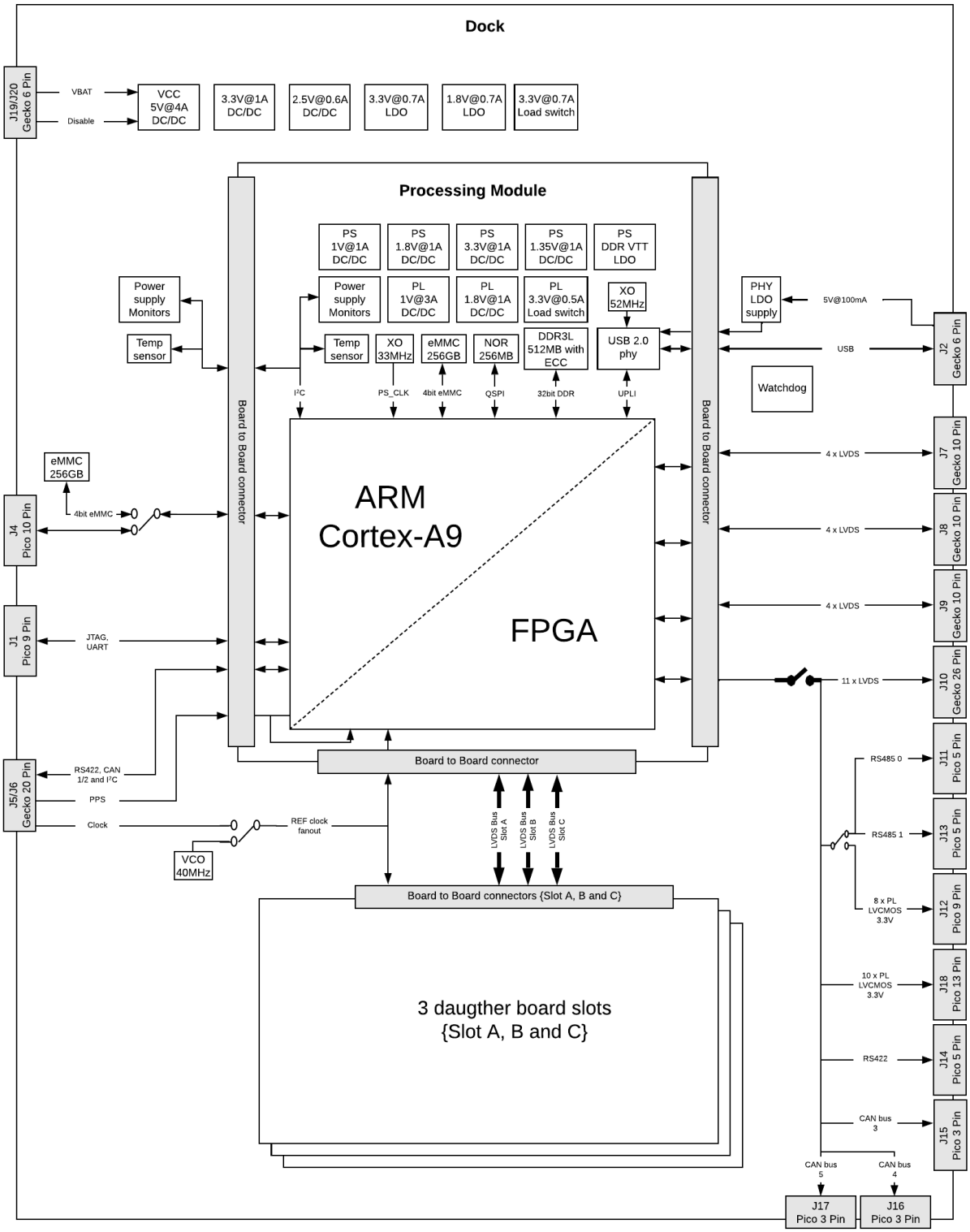

Figure 3.1: NanoCom SDR MK3 Block diagram

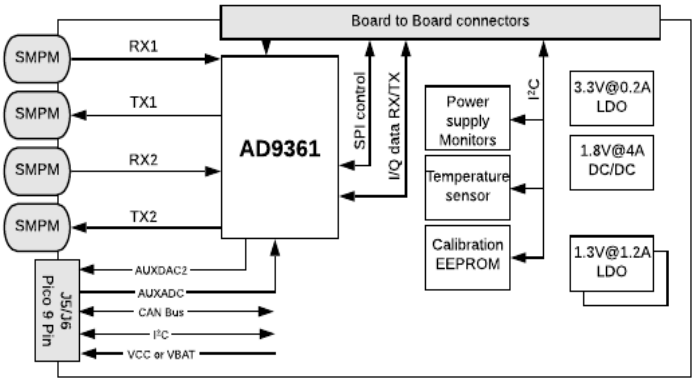

Figure 3.2: TR600 block diagram

4 Thermal Characteristics

The thermal interface of the unit is defined on the mechanical connection point marked with red square in Figure 4.1.
The NanoCom SDR MK3 has been qualified with three TR600 modules to an operational temperature range from -40°C to 50°C and a non-operational temperature range from -40°C to 85°C.

The most critical circuit has a maximum operational temperature of 85°C. At an interface temperature of 53°C, the most critical circuit temperature is 82°C at maximum operational power, so a maximum interface temperature 50°C gives sufficient margin to ensure that the most critical circuit is below 85°C.

Higher interface temperatures can be tolerated if it is ensured that the different modules all remain below 85°C.

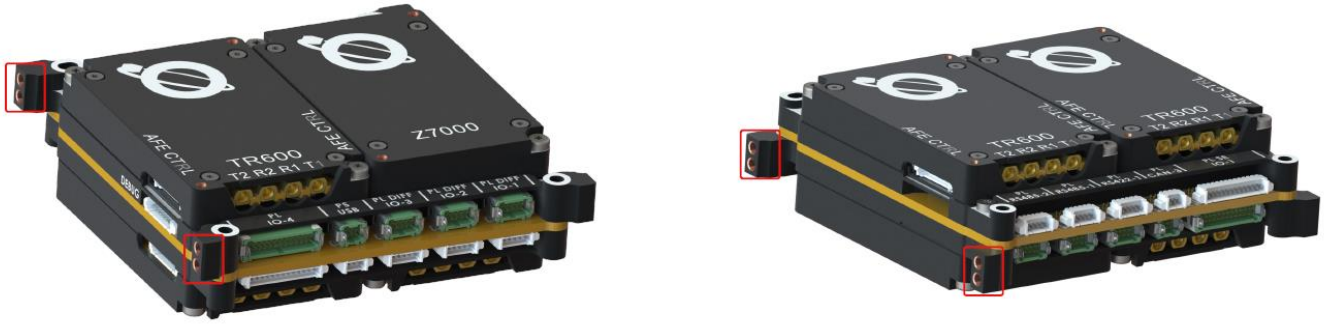

Figure 4.1: Thermal interface

5 Mechanical Characteristics

The NanoCom SDR MK3 is equipped with one, two or three TR-600 depending on the purchased configuration. Perspective views of the different configurations are shown below.

Figure 5.1: NanoCom SDR MK3 Option one TR600

TR600 Slot A
Slot B and C Empty

Figure 5.2: NanoCom SDR MK3 Option two TR600

TR600 Slot A and B
Slot C Empty

Figure 5.3: NanoCom SDR MK3 Option three TR600

TR600 Slot A, B and C

Description	Value	Unit
Mass total with 1xTR600 (typical)	272	g
Mass total with 2xTR600 (typical)	306	g
Mass total with 3xTR600 (typical)	342	g
Size with 1xTR600 (L x W x H)	95 x 95 x 23,85	mm
Size with 2xTR600 (L x W x H)	95 x 95 x 31,65	mm
Size with 3xTR600 (L x W x H)	95 x 95 x 31,65	mm

Table 5.1: Mechanical properties

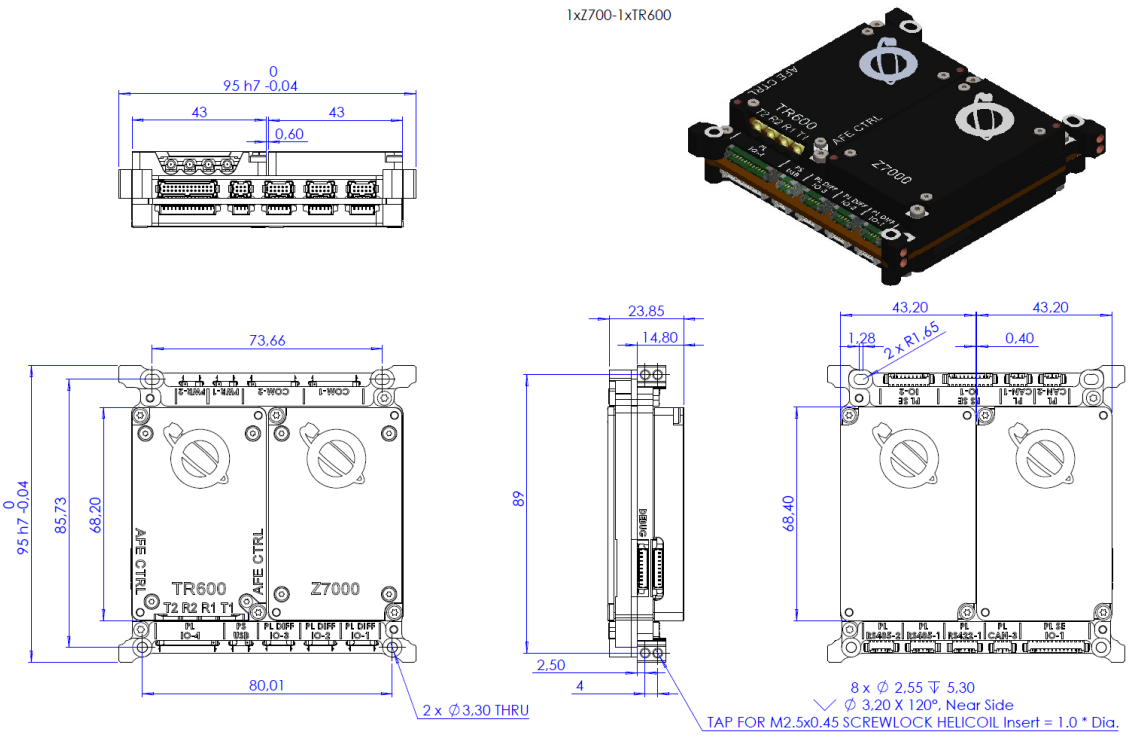

Figure 5.4: NanoCom SDR MK3 with 1xTR600 mechanical drawing (all dimensions are in mm)

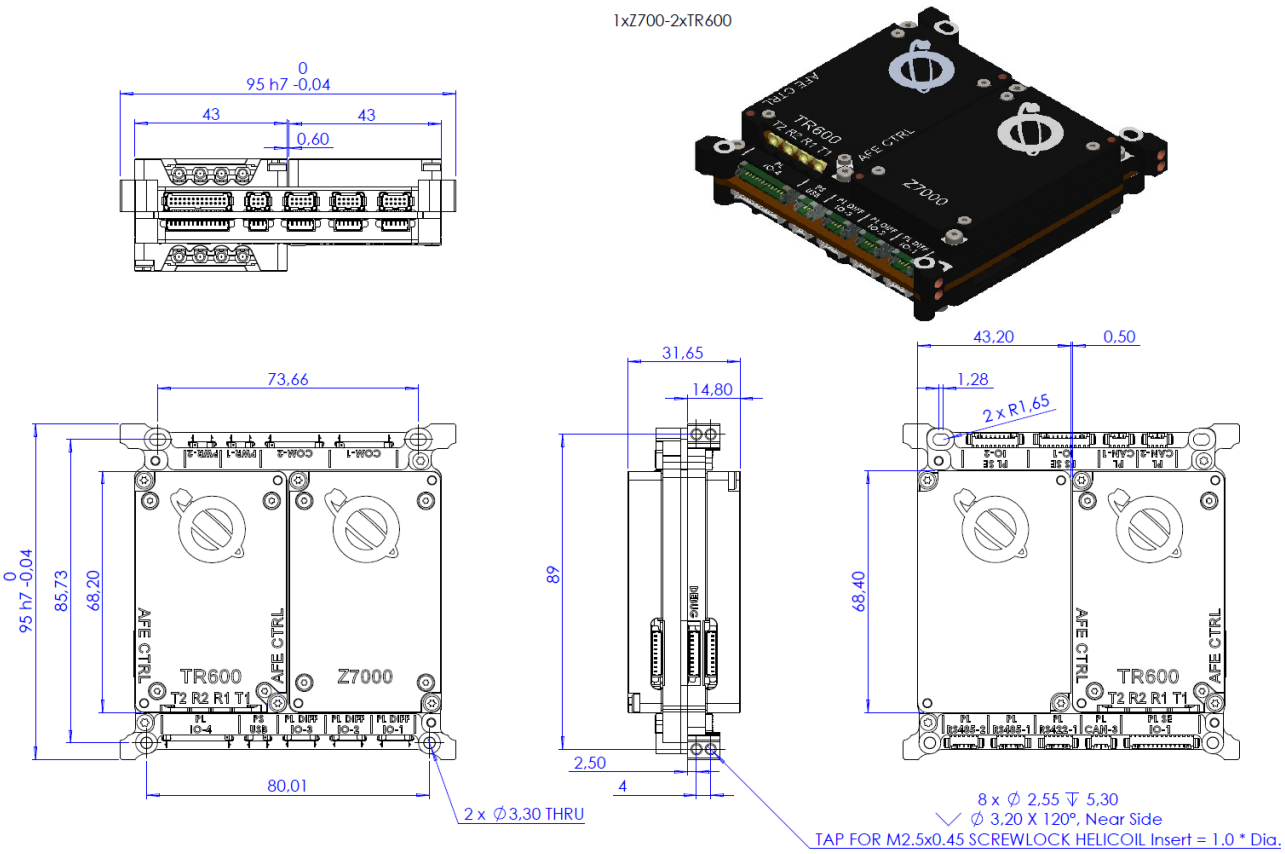

Figure 5.5: NanoCom SDR MK3 with 2xTR600 mechanical drawing (all dimensions are in mm)

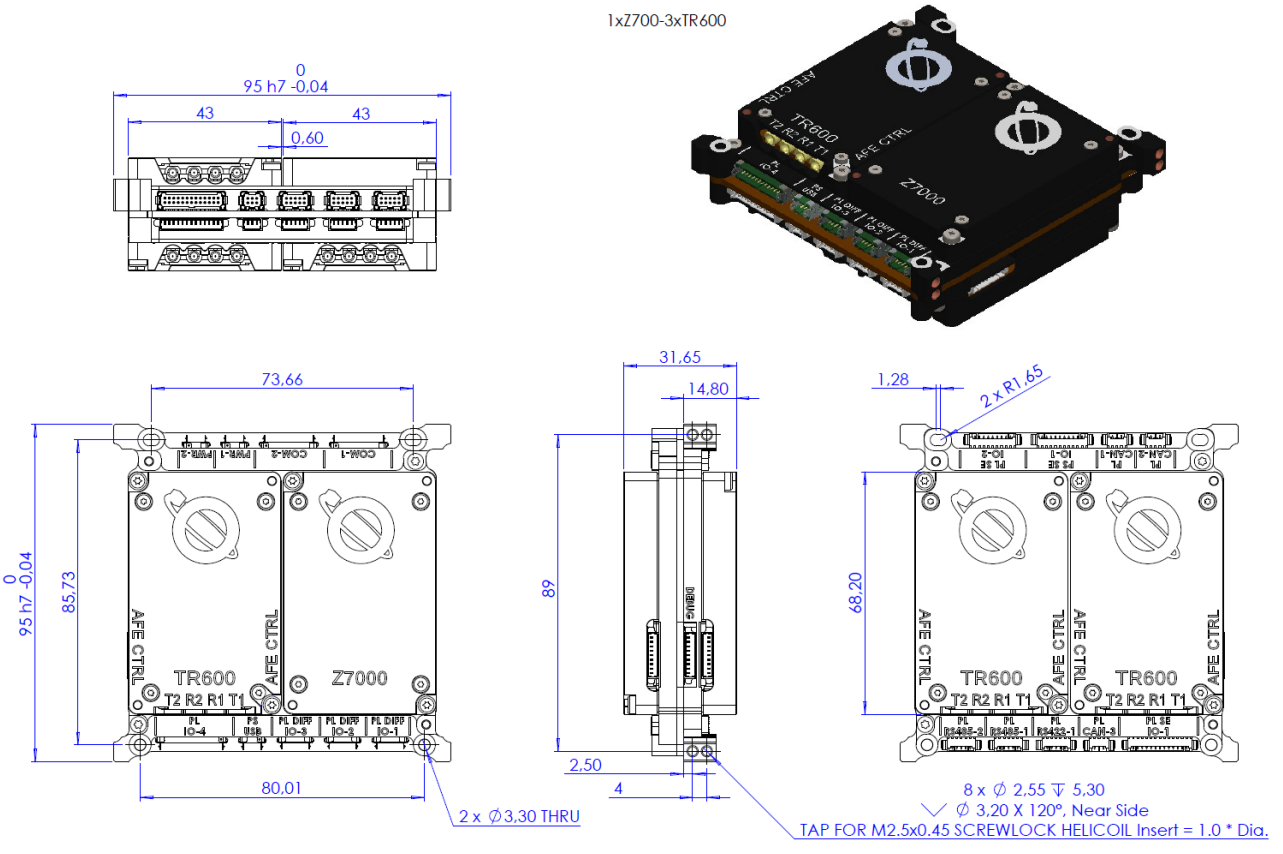

Figure 5.6: NanoCom SDR MK3 with 3xTR600 mechanical drawing (all dimensions are in mm)

6 Connectors overview

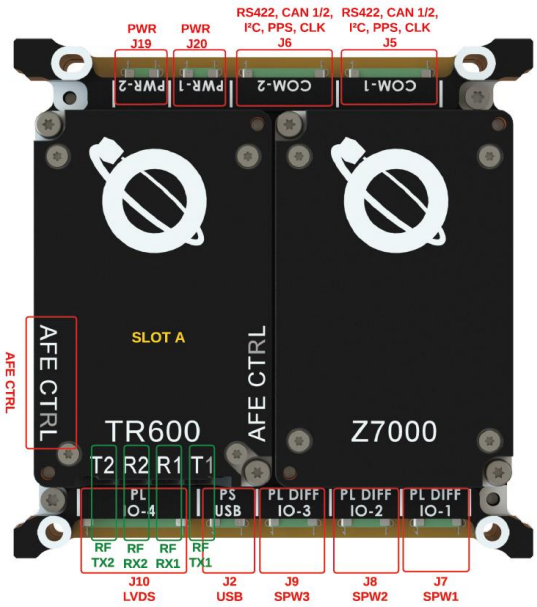

Figure 6.1: NanoCom SDR MK3 top view

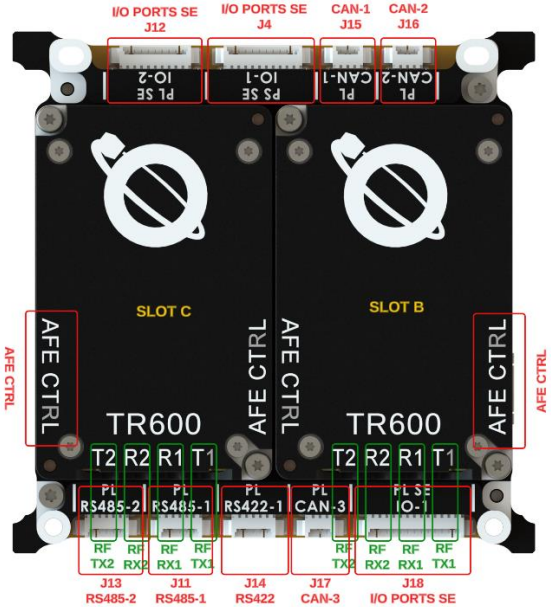

Figure 6.2: NanoCom SDR MK3 bottom view

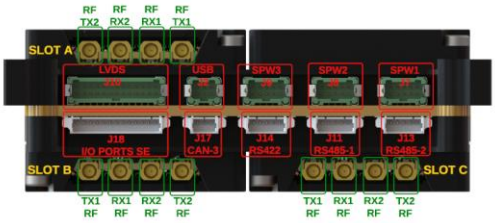

Figure 6.3: NanoCom SDR MK3 front view

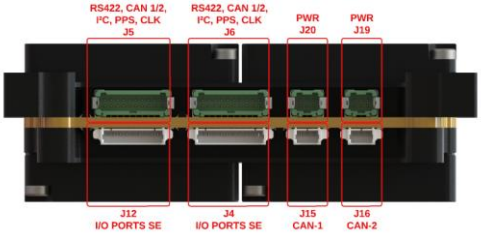

Figure 6.4: NanoCom SDR MK3 back view

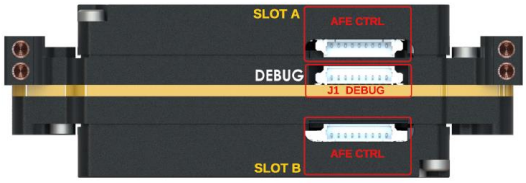

Figure 6.5: NanoCom SDR MK3 left side view

Figure 6.6: NanoCom SDR MK3 right side view

7 Included Cable kit

Cables necessary for interfacing with the NanoCom SDR MK3 product for initial bring-up are included with the product. This includes power cables and main interfaces. Below is an overview of cables included with the product for debug/test purpose only:

Name	Connection NanoCom	Connection Breakout PCB	GomSpace ID	Length	Description
PWR	PWR-1 (J20) or PWR-2 (J19)	-	110448	50cm	Power harness to flying leads
DB1	DEBUG (J1)	J2	108562	3.5cm	Debug harness
DB2	-	-	108558	N.A.	Debug breakout PCB
DB3	-	J5	103011	N.A.	FTDI USB-TTL serial cable
DB4	-	J3	104557	1200 cm	JTAG-HS3 & USB A to MICRO USB B
USB	USB (J2)	-	108560	1000 cm	USB Cable
Main Bus	COM-1 (J5) or COM-2 (J6)	-	108559	15 cm	Main Bus Harness Flying Leads
RF connection	TX1, RX1, TX2, RX2 on TR600 module	-	108733	15 cm	RF cable for connection to SMA male
RF connection	TX1, RX1, TX2, RX2 on TR600 module	-	108732	15 cm	RF cable for connection to SMA female

Table 7.1: Product cable kit content

The location of the required individual connectors is documented below.

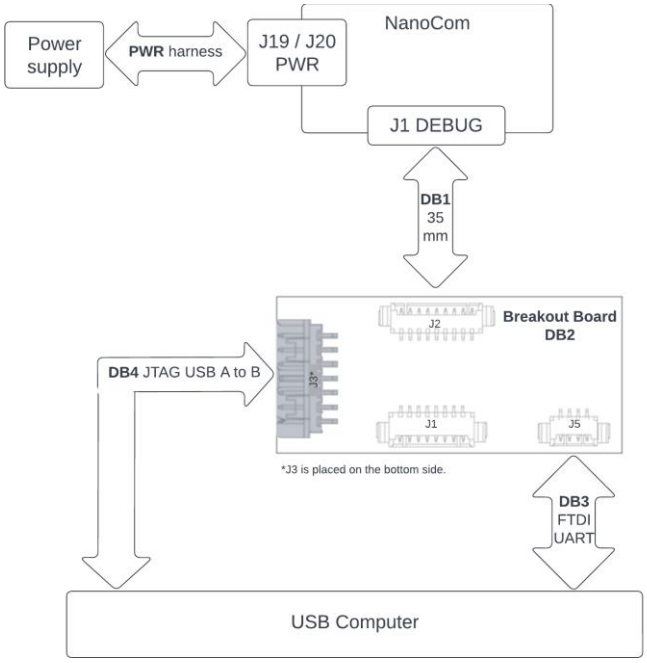

Figure 7.1: Breakout board and connections for develop and debugging

8 Electrical Characteristics

8.1 Power Characteristics

The current value in the Table 8.1 below was measured with a SDR with three TR600 and Zynq 7045 at 25°C.

Parameter	Condition	Min	Typ	Max	Unit
Supply Current (Main/Backup), in Idle[1]	V_{in} = 12V, 25°C		185		mA
	V_{in} = 18V, 25°C		125		mA
	V_{in} = 24V, 25°C		100		mA
	V_{in} = 32V, 25°C		80		mA
Supply Current (Main/Backup), enable one TR600 on Slot A[2]	V_{in} = 12V, 25°C		455		mA
	V_{in} = 18V, 25°C		310		mA
	V_{in} = 24V, 25°C		237		mA
	V_{in} = 32V, 25°C		184		mA
Supply Current (Main/Backup), enable two TR600 on Slot A and Slot B[2]	V_{in} = 12V, 25°C		595		mA
	V_{in} = 18V, 25°C		398		mA
	V_{in} = 24V, 25°C		302		mA
	V_{in} = 32V, 25°C		232		mA
Supply Current (Main/Backup), enable three TR600 on Slot A, Slot B and Slot C[2]	V_{in} = 12V, 25°C		730		mA
	V_{in} = 18V, 25°C		485		mA
	V_{in} = 24V, 25°C		366		mA
	V_{in} = 32V, 25°C		280		mA

Table 8.1: Current consumption values

[1] Linux running in idle, default after startup, no PL services running, no external devices.

[2] TR600(s) are powered-on (PL activated) without any transmitting data and no external devices.

8.2 Interfaces Characteristics

Interface	Connector	Parameter	Min	Typ	Max	Unit
V_{in}	J19, J20	Supply voltage (Main/Backup)	12		32	V
SpaceWire /LVDS	J7, J8, J9, J10	Differential input voltage	100	350	600	mV
		Common mode input voltage	0.30	1.20	1.5	V
		Differential output voltage	247	350	600	mV
		Common mode output voltage	1.00	1.25	1.425	V
CAN	J5, J6, J15[1], J16[1], J17[1]	Differential input threshold voltage	0.50		0.90	V
		Common mode input voltage			±25	V
		Differential output threshold voltage (recessive)	-500	0	50	mV
		Differential output threshold voltage (dominant)	1.5	2.2	3.0	V
		Common mode output voltage (dominant)	1.45	1.95	2.45	V
RS422[2]/ RS485[2]	J5, J6, J11, J13, J14	Differential Input Threshold	-0.20		0.20	V
		Receiver input voltage range	0		4	V
		Differential output voltage	2.0			V
		Common mode output voltage			3	V
CLK	J5, J6	Differential input voltage		150		mV
		Common mode input voltage	1.55		1.7	V
I2C	J5, J6	Input logic high voltage		3.3		V
		SDA, SCL Logic input threshold voltage	1.6	1.8	2	V
		Input logic low voltage			0.4	V
		Output logic high voltage		3.30		V
		Output logic low voltage	0	0.19	0.3	V
PPS	J5, J6	Logic power supply voltage		3.3		V
		Differential Input Voltage	0.10		0.60	V
		Common mode input range	0.05		2.45	V

Table 8.2: Input and output characteristics

Interface	Connector	Parameter	Min	Typ	Max	Unit
IO	J4, J12, J18	High-level input voltage	2.15	3.30	3.30	V
		Low-level input voltage	0	0	0.8	V
	J4	High-level output voltage, @ -16mA	2.90	3.30		V
		Low-level output voltage @ 16mA		0	0.4	V
		Maximum output current[3]	-16		16	mA
	J12[4], J18[4]	High-level output voltage, @ -20uA	2.90	3.30		V
		Low-level output voltage @ 20uA		0	0.4	V
		Maximum output current	-20		+20	uA
ADC	AFE CTRL	Resolution		12		Bits
DAC	AFE CTRL	Resolution		10		Bits

Table 8.3 : Input and output characteristics (following)

[1] Need PL license for implementation, see section 9.10 for more details.

[2] The RS422 and RS485 input with 120Ω differential termination between RS4xx-RX-P and RS4xx-RX-N terminals. For failsafe operation the differential input is equipped with a resistive divider network to terminate the input of the RS4xx transceiver when nothing is connected. The resistive network consists of a 390Ω pullup via a Schottky diode to 3.3V supply and a 390Ω pulldown to GND (see Figure 8.1 below).

[3] SoC configurable to supported drive strengths of 4, 8, 12, or 16 mA.

[4] It can only translate push-pull CMOS logic outputs.

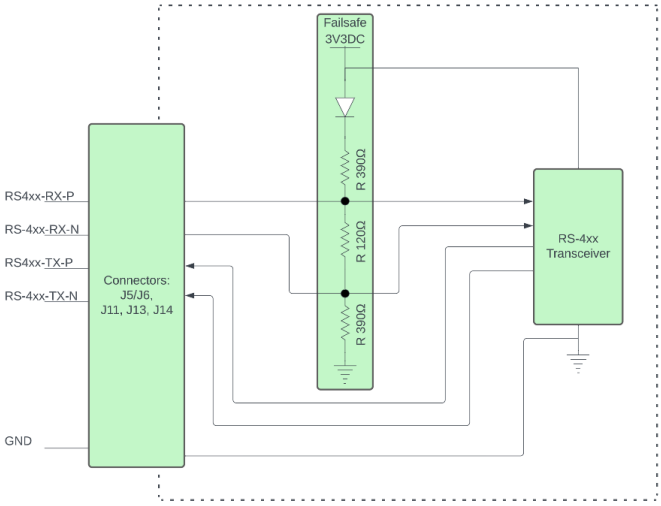

Figure 8.1: RS422 and RS485 interface

9 Connectors and Pin Functions

9.1 PWR-1 and PWR-2 (J19, J20)

NanoCom SDR MK3 is equipped with two Harwin Gecko G125-MH10605L1R 1.25mm pitch high-reliability connectors, with latches, for external power supply. The board can be supplied through either connector, PWR-1 or PWR-2, using a single power supply or by connecting two independent power supplies for redundancy. A supply balancing circuit automatically selects whichever of the two power connectors that carries the highest VIN voltage as supply source. The load will be shared between the two power connectors if the external supply voltages VIN1 and VIN2 are of equal levels.

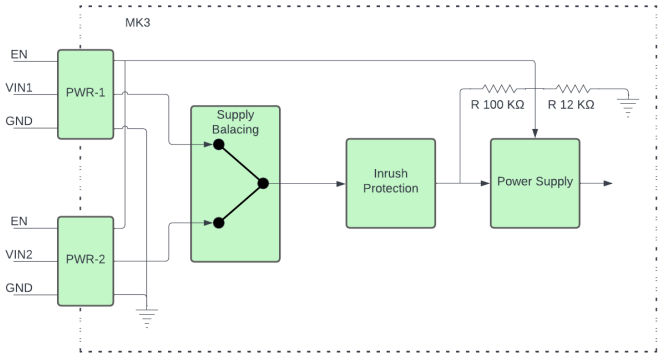

Figure 9.1: NanoCom SDR MK3 power supply interface

The EN pin makes it possible to turn ON or OFF the SDR MK3 independent of supply voltage. The feature can be omitted by leaving the EN pin not connected. When the EN pin is left floating / not connected, the SDR MK3 will automatically turn ON when the supply voltage raises above 10V and turn OFF below at supply voltages below 8.5V. The EN pins from PWR-1 and PWR-2 are internally connected.

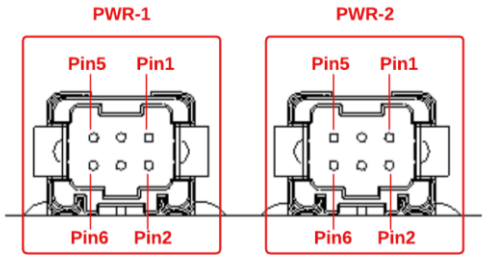

Figure 9.2: PWR-1 and PWR-2 pinout

Pin	PWR-1 Signal	PWR-2 Signal	Description
1	VIN1	VIN2	Supply voltage VCC (12V to 32V)
2	EN	EN	Optional enable signal, tied to Vin through a 100kohm / 12kohm divider locally on the SDR MK3. EN = 0V to 0.8V: SDR MK3 is OFF EN = 1.2V to 24V: SDR MK3 is ON EN = Not connected: Automatic supply switching, SDR MK3 is ON when supply voltage is > 10V and OFF < 8.5V
3	VIN1	VIN2	Supply voltage VCC (12V to 32V)
4	GND	GND	Ground
5	VIN1	VIN2	Supply voltage VCC (12V to 32V)
6	GND	GND	Ground

Table 9.1: PWR-1 and PWR-2 pin allocation

9.2 CAN and RS422 - COM 1-2 (J5, J6)

NanoCom SDR MK3 is equipped with two Harwin Gecko G125-MH12005L1R 1.25mm pitch high-reliability connectors, with latches, for access to its main communication interface. The individual pins of the two connectors are interconnected, which allow the NanoCom SDR to use with in different bus topologies. The secondary connector can be used for interconnecting with other devices in multidrop bus configuration or for bus terminations if it is the last node in the system.

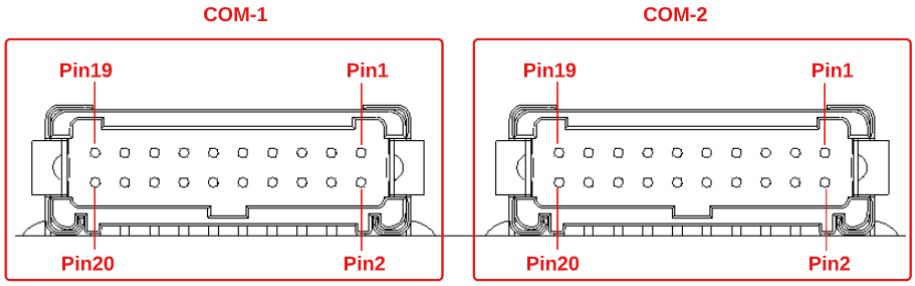

Figure 9.3: COM-1 and COM-2 pinout

Pin	Signal	Description
1	I2C-SDA	I2C serial data line[1] [5]
2	CAN1_H	CAN1 High[2]
3	GND	Ground
4	CAN1_L	CAN1 Low[2]
5	I2C-SCL	I2C serial clock line[1] [5]
6	CAN2_H	CAN2 High[2] [5]
7	GND	Ground
8	CAN2_L	CAN2 Low[2] [5]
9	PPS-P	Pulse Per Second LVDS positive input line[3]
10	CLK-P	External reference clock LVDS positive input line
11	PPS-N	Pulse Per Second LVDS negative input line[3]
12	CLK-N	External reference clock LVDS negative input line
13	NC	Not connected
14	RS422-TX-P	RS422 Noninverting driver output for payload data interface
15	GND	Ground
16	RS422-TX-N	RS422 Inverting driver output for payload data interface
17	NC	Not connected
18	RS422-RX-P	RS422 Noninverting receiver input for payload data interface[4]
19	GND	Ground
20	RS422-RX-N	RS422 Inverting receiver input for payload data interface[4]

Table 9.2: COM-1 and COM-2 pin allocation

[1] There are no internal discrete pull-up resistors. Multi-master/CSP not supported by SW drivers, only connect slave devices.

[2] CAN1 and CAN2 are without any differential termination between CAN_H and CAN_L.

[3] No discrete termination, 100Ω resistor shall be added between PPS-P and PPS-N if used.

[4] Discrete 120Ω termination between RS422-RX-P and RS422-RX-N and discrete pull-up/pull-down termination for failsafe operation, see Figure 8.1.

[5] Also connected to AFE CTRL, see §9.13 for more details.

9.3 SpaceWire – PL DIFF 1-3 (J7, J8, J9)

NanoCom SDR MK3 is equipped with three independent bi-directional, full-duplex SpaceWire interfaces for payload data transfer. It uses Gecko G125-MH11005L1R 1.25mm pitch high-reliability connectors, with latches from Harwin for each of the three interfaces:

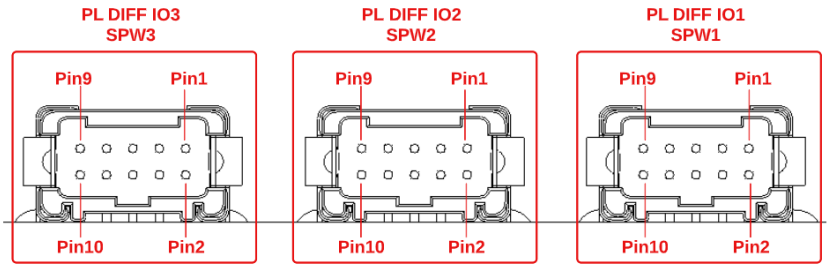

Figure 9.4: SPW1, SPW2 and SPW3 pinout

Each SpaceWire[1] interface uses two signals, data and strobe, in receive and transmit direction to send serial bit streams. The signals are based on low voltage differential signals according to the ANSI TIA/EIA-644 Standard and require two pins for each signal.

The electrical interface is a protected switch. To enable it, set a logic HIGH on SoC pin: Y17 for J7; AA17 for J8 and W17 for J9. By default, this interface is disabled (pull-down resistor on each pin Y17, AA17, W17).

Connector Pin	Signal	Description	SoC pin (J7)	SoC pin (J8)	SoC pin (J9)
1	Dout-	LVDS Data output negative line	AD15	AB16	W15
2	Sin+	LVDS Strobe input positive line[2]	AC13	AF15	AC17
3	Dout+	LVDS Data output positive line	AD16	AB17	W16
4	Sin-	LVDS Strobe input negative line[2]	AD13	AF14	AC16
5	GND	Ground connection for internal cable shielding[3]			
6	GND	Ground connector for external cable shielding[3]			
7	Sout-	LVDS Strobe output negative line	AB14	AF17	Y15
8	Din+	LVDS Data input positive line[2]	AC14	AE16	AA15
9	Sout+	LVDS Strobe output positive line	AB15	AE17	Y16
10	Din-	LVDS Data input negative line[2]	AD14	AE15	AA14

Table 9.3: SPW-1, SPW-2 and SPW-3 pin allocation

[1] Can be repurposed for other protocols through development kit.

[2] Differential 100Ω termination resistor configurable in the SoC.

[3] Two pins for internal and external cable shielding are provided as well in each SpaceWire interface. A SpaceWire cable contains four twisted pair of wires with a characteristic impedance of 100Ω. In case of shielding, it is possible to uses those pins to terminate internally (around each twisted pair) and externally shielding by connecting to those pins.

9.4 PL Differential Input/Output – PL IO-4 (J10)

NanoCom SDR MK3 is equipped with 11 Low Volage Differential Signaling (LVDS) pairs used for general purpose. It uses a Gecko G125-MH12605L1P 1.25mm pitch high-reliability connector, with latches from Harwin:

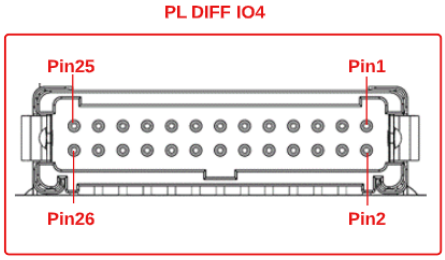

Figure 9.5: PL DIFF IO-4 LVDS pinout

These pins are unused in the GomSpace provided reference design but can be configured with the development kit. Differential 100Ω input termination resistor can be configured in the SoC.

The electrical interface is a protected switch. To enable it, set a logic HIGH on W14 SoC pin. By default, this interface is disabled (pull-down resistor on W14).

Connector Pin	Signal	Description	SoC pin
1	LVDS1-P	LVDS1 positive line	Y10
2	GND	Ground	
3	LVDS1-N	LVDS1 negative line	AA10
4	LVDS2-P	LVDS2 positive line	AE13
5	LVDS3-P	LVDS3 positive line	AB11
6	LVDS2-N	LVDS2 negative line	AF13
7	LVDS3-N	LVDS3 negative line	AB10
8	GND	Ground	
9	LVDS4-N	LVDS4 negative line	Y11
10	LVDS5-P	LVDS5 positive line	AE12
11	LVDS4-P	LVDS4 positive line	Y12
12	LVDS5-N	LVDS5 negative line	AF12
13	LVDS6-P	LVDS6 positive line	AB12
14	LVDS7-P	LVDS7 positive line	AE11
15	LVDS6-N	LVDS6 negative line	AC11
16	LVDS7-N	LVDS7 negative line	AF10
17	GND	Ground	
18	LVDS8-P	LVDS8 positive line	AE10
19	LVDS9-P	LVDS9 positive line	W13
20	LVDS8-N	LVDS8 negative line	AD10
21	LVDS9-N	LVDS9 negative line	Y13
22	LVDS10-P	LVDS10 positive line	AA13
23	LVDS11-P	LVDS11 positive line	AC12
24	LVDS10-N	LVDS10 negative line	AA12
25	LVDS11-N	LVDS11 negative line	AD11
26	GND	Ground	

Table 9.4 : PL DIFF IO-4 LVDS pin allocation

9.5 PL Single Ended Input/Output 1– PL SE IO-1 (J18)

NanoCom SDR MK3 is equipped with 10 single-ended (SE) input/output used for general purpose. It uses a Picoblade 532611371 1.25mm pitch high-reliability connector from Molex:

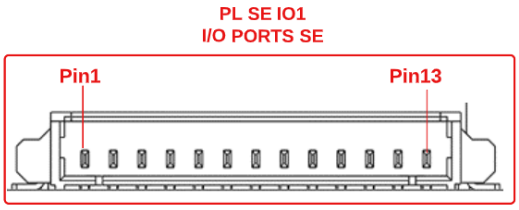

Figure 9.6: PL SE IO-1 pinout

These pins are unused in the GomSpace provided reference design but can be configured with the development kit.

The electrical interface is a bidirectional buffer, it is always available.

Connector Pin	Signal	Description	SoC pin
1	GND	Ground	
2	IO1	SE Input/Output 1	V19
3	IO2	SE Input/Output 2	V18
4	IO3	SE Input/Output 3	AE25
5	IO4	SE Input/Output 4	AE22
6	IO5	SE Input/Output 5	AF22
7	GND	Ground	
8	IO6	SE Input/Output 6	AE23
9	IO7	SE Input/Output 7	AD21
10	IO8	SE Input/Output 8	AC21
11	IO9	SE Input/Output 9	AC22
12	IO10	SE Input/Output 10	AF20
13	GND	Ground	

Table 9.5: PL SE IO-1 pin allocation

9.6 PL Single Ended Input/Output 2– PL SE IO-2 (J12)

NanoCom SDR MK3 can be equipped with additional 8 single-ended (SE) input/output used for general purpose if RS485 is not used (on J11, J13). It uses a Picoblade 532610971 1.25mm pitch high-reliability connector from Molex:

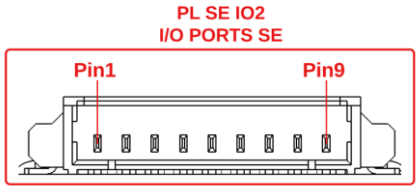

Figure 9.7: PL SE IO-2 pinout

These pins (Table 9.6 in next pages) are unused in the GomSpace provided reference design but can be configured with the development kit. By hardware design, J12 is enabled and RS485 is disabled.

The electrical interface is a bidirectional buffer. To enable J12, set a logic LOW on Y18 SoC pin (auto-disable J11 and J13 interfaces). Set a logic HIGH to use RS485 on J11 and J13 (auto-disable J12). Signals from J12 pins 1 to 4 are also connected to J11. Signals from J12 pins 6 to 9 are also connected to J13.

Connector Pin	Signal	Description	SoC pin
1	IO1	SE Input/Output 1	AD19[1]
2	IO2	SE Input/Output 2	AF18[1]
3	IO3	SE Input/Output 3	AE18[1]
4	IO4	SE Input/Output 4	AD18[1]
5	GND	Ground	
6	IO5	SE Input/Output 5	AB20[2]
7	IO6	SE Input/Output 6	AC19[2]
8	IO7	SE Input/Output 7	AC18[2]
9	IO8	SE Input/Output 8	AA20[2]

Table 9.6: PL SE IO-2 pin allocation

9.7 PS Single Ended Interface – PS SE IO-1 (J4)

NanoCom SDR MK3 is equipped with 6 single-ended Multiplexed Input/Output (MIO) used for general purpose. It uses a Picoblade 532611071 1.25mm pitch high-reliability connector from Molex:

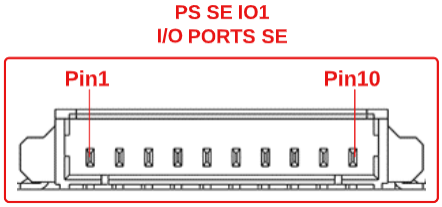

Figure 9.8: PS SE IO-1 pinout

These pins are unused in the GomSpace provided reference design but can be configured with the development kit. The MIO is shared with the secondary eMMC and cannot be used while this is active.

The electrical interface is a multiplexed switch. To enable this interface, set a logic LOW on G21 SoC pin (which disables the use of eMMC). By default, this interface is enabled (pull-down resistor on G21).

Connector Pin	Signal	Description	SoC pin
1	IO1	Multiplexed Input/Output 1	C22
2	GND	Ground	
3	IO2	Multiplexed Input/Output 2	C19
4	GND	Ground	
5	IO3	Multiplexed Input/Output 3	C18
6	GND	Ground	
7	IO4	Multiplexed Input/Output 4	F17
8	GND	Ground	
9	IO5	Multiplexed Input/Output 5	D18
10	IO6	Multiplexed Input/Output 6	E18

Table 9.7: PS SE IO-1 pin allocation

9.8 RS485 interfaces – PL RS485 1-2 (J11, J13)

NanoCom SDR MK3 is equipped with two full duplex RS485 interfaces. It uses a Picoblade 532610571 1.25mm pitch high-reliability connector from Molex:

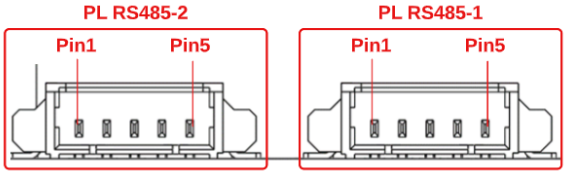

Figure 9.9: RS485 pinout

PL SE IO-2 (J12) and RS485 (J11, J13) connectors are mutually exclusive. By default, RS485 is configured for use in the SoC. The driver feature fullduplex communication and it is not compatible to half-duplex.

Pin	Signal	Description
1	RS485-TX-N	RS485 Drive Negative
2	RS485-TX-P	RS485 Drive Positive
3	GND	Ground
4	RS485-RX-N	RS485 Receive Negative[1]
5	RS485-RX-P	RS485 Receive Positive[1]

Table 9.8: RS485 pin allocation

[1] Discrete 120Ω termination between RS485-RX-P and RS485-RX-N and discrete pull-up/pull-down termination for failsafe operation, see Figure 8.1.

9.9 RS422 interface – PL RS422-1 (J14)

NanoCom SDR MK3 is equipped with a full duplex RS422 interface. It uses a Picoblade 532610571 1.25mm pitch high-reliability connector from Molex:

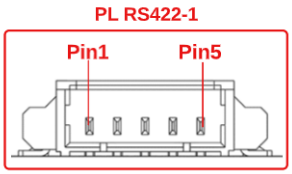

Figure 9.10: RS422 pinout

These pins can only be used for RS422 interface. The driver feature fullduplex communication and it is not compatible to half-duplex.

Pin	Signal	Description
1	RS422-TX-N	RS422 Drive Negative
2	RS422-TX-P	RS422 Drive Positive
3	GND	Ground
4	RS422-RX-N	RS422 Receive Negative[1]
5	RS422-RX-P	RS422 Receive Positive[1]

Table 9.9: RS422 pin allocation

[1] Discrete 120Ω termination between RS422-RX-P and RS422-RX-N and discrete pull-up/pull-down termination for failsafe operation, see Figure 8.1.

9.10 PL CAN 1-3 * (J15, J16, J17)

NanoCom SDR MK3 is equipped with three hardware CAN interfaces. It uses a Picoblade 532610371 1.25mm pitch high-reliability connector from Molex:

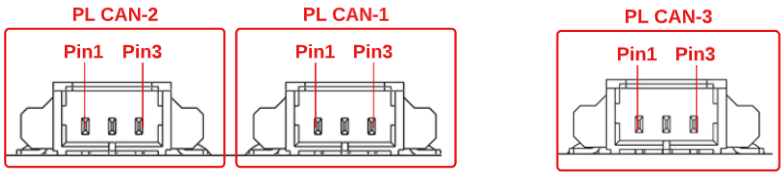

Figure 9.11. CAN pinout

These interfaces are reserved for future use. The IP cores realizing the protocol are not delivered by GomSpace but may be added through the provided development kit. It furthermore requires a proper license agreement with Robert Bosch.

Pin	Signal	Description
1	CAN_H	CAN High[1]
2	CAN_L	CAN Low[1]
3	GND	Ground

Table 9.10: CAN pin allocation

[1] CAN-1 has 120R differential termination between CAN_H and CAN_L. CAN-2 and CAN-3 are without any differential termination between CAN_H and CAN_L.

9.11 Debug and Programming Interface – DEBUG (J1)

NanoCom SDR MK3 is equipped with a debug connector including JTAG, UART and Reset. It uses a Picoblade 532610971 1.25mm pitch high-reliability connector from Molex:

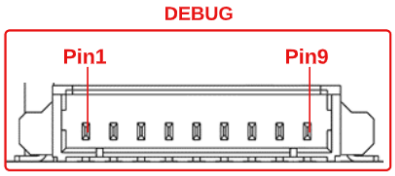

Figure 9.12: Debug and programming pinout

The debug and programming interface is used for development and debugging. The interface is not intended to be used in flight or integrated with the satellite bus.

Pin	Signal	Description
1	TDO	JTAG Test Data Out
2	TCK	JTAG Test Clock
3	TMS	JTAG Test Mode Select
4	TDI	JTAG Test Data In
5	SYS_RST	System Reset
6	3.3V	3.3V from the NanoCom SDR[1]
7	UART_RX	Debug UART DUT Receive Line
8	UART_TX	Debug UART DUT Transmit Line
9	GND	Ground

Table 9.11: DEBUG pin allocation

[1] Maximum output continuous current is +/- 25mA.

9.12 PS USB (J2)

NanoCom SDR MK3 is equipped with a Harwin Gecko G125-MH10605L1R 1.25mm pitch high-reliability connectors, with latches, for USB interface.

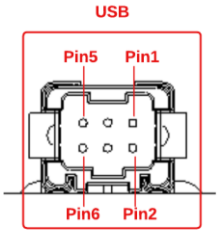

Figure 9.13: USB pinout

The NanoCom SDR MK3 supports USB 2.0 device and host[1] application on the dedicated USB connector.

Pin	Signal	Description
1	VBUS_IN	USB VBUS 5V input
2	USB D-	USB Data negative
3	VBUS_OUT[1]	USB VBUS 4.6V output – Only for host application. Left unconnected for device application.
4	USB D+	USB Data positive
5	GND	Ground
6	GND	Ground

Table 9.12: USB pin allocation

[1] For host application, connect VBUS_OUT to VBUS_IN. The maximum host VBUS voltage is 4.6V.

9.13 AFE CTRL Interfaces

On both sides of the TR600 modules a nine-pin Picoblade connector, 532610971 1.25mm pitch high-reliability connector from Molex, is present with interface connections options to an external RF Front End. It contains CAN_P/N, I²C SCL/SDA as communication interface, power supply, a 10-bit AUXADC and AUXDAC2.

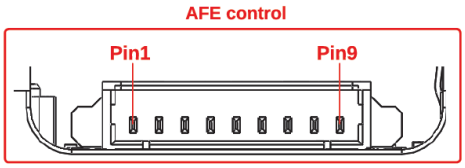

Figure 9.14. AFE CTRL TR600 pinout

Pin	Signal	Description
1	CAN2_H	CAN2 High[1]
2	CAN2_L	CAN2 Low[1]
3	GND	Ground
4	I2C-SCL	I2C serial clock line[2]
5	I2C-SDA	I2C serial data line[2]
6	PSU	Output 4.6V power supply[3]
7	AUXDAC2	Directly connected to the TR600 transceiver (AD9361-AUXDAC2)
8	AUXADC	Directly connected to the TR600 transceiver (AD9361-AUXADC)
9	GND	Ground

Table 9.13: AFE CTRL TR600 pin allocation

[1] Directly connected to CAN2 on COM -1-2 (J5/J6), see §9.2 for hardware details.

[2] Connected to I2C on COM-1-2 with an address translator, the translation byte for each slot is: Slot A: 0x40, Slot B: 0x58, Slot C: 0x51. See §9.2 for hardware details.

[3] Maximum output current is 200mA. ON/OFF controlled by GPO_0 of the AD9361.

9.14 AFE CTRL through RF connector (RX1/2, TX1/2)

The four RF antenna connectors have added functionality for superimposing a DC signal on top of the RF signals. The two RF RX coax can be connected to PSU[1] by the ON/OFF controlled with GPO1 of the TR600 transceiver (AD9361). The two RF TX can be used as digital pin controller by using GPO2 (on TX1) and GPO3 (on TX2) of the transceiver.

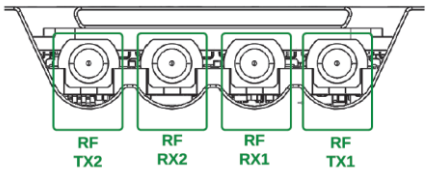

Figure 9.15: RF connectors

[1] Maximum output current is 200mA.

10 Performance Characteristics

10.1 eMMC

The eMMC performance characteristics are derived using the "fio" https:/fio.readthedocs.io/en/latest/fio_doc.html benchmarking application. Below tables summarize varying workloads for read, write and simultaneous read/write operations of a single eMMC instance.

Sequential Read	Sequential Write	Sequential Read/write
23 MByte/sec (22 IOPS)	21 MByte/sec (20 IOPS)	11/11 MByte/sec (10/10 IOPS)

Random Read	Random Write	Random Read/write
22 MByte/sec (21 IOPS)	21 MByte/sec (20 IOPS)	11/11 MByte/sec (10/10 IOPS)

Table 10.1: eMMC performances

Striped storage can be achieved by utilizing both eMMC instances in parallel and thus reaching an improved performance.

Sequential Read	Sequential Write	Sequential Read/write
45 MByte/sec (42 IOPS)	41 MByte/sec (38 IOPS)	20/20 MByte/sec (20/20 IOPS)

Random Read	Random Write	Random Read/write
47 MByte/sec (45 IOPS)	43 MByte/sec (41 IOPS)	22/22 MByte/sec (21/21 IOPS)

Table 10.2: Striped eMMC performances

10.2 SpaceWire

The SpaceWire performance characteristics are derived using the "iperf3" (https://iperf.fr/iperf-doc.php) benchmarking application. The benchmark is thus conducted at the network layer with an MTU of 9000 bytes. Below table summarize the performance for both a single interface and three interfaces transferring data.

	TCP/UDP
Single interface (unidirectional)	150 Mbit/sec
Three interfaces (unidirectional)	150 Mbit/sec
Three interfaces (bidirectional)	80 Mbit/sec

Table 10.3: SpaceWire characteristics

10.3 RS-422

The RS-422 performance characteristics are derived using the "iperf3" (https://iperf.fr/iperf-doc.php) benchmarking application. The test is thus conducted at the network layer and below table summarize the performance for each of the two interfaces for TCP transfers.

PS	PL
3 Mbit/sec	2.2 Mbit/sec

Table 10.4: RS-422 characteristics

10.4 RF Characteristics

The NanoCom SDR MK3 can be equipped with up to three TR600 modules. The TR600 modules are identical with regards to RF performance. The three TR600 modules are placed one in each slot A, B and C.
The RF characteristics for the TR600 modules is presented as typical measurements as the module can be configured to an endless set of different configurations. Only a small subset is presented in this datasheet.

Each TR600 consists of two identical and independently controlled TX channels for direct conversion sharing a common frequency synthesizer.

The RF receivers contain two independent RX channels for direct down conversion sharing a common frequency synthesizer.

10.4.1 TX Power

The output power of the TR-600 is controlled by a hardware gain setting in the transceiver, which will be called the *power setting* in this datasheet.

In this section, the power setting is swept while the output power is recorded to check the linearity of the power control. Any compression at high power settings will also be revealed. The transfer function is defined as:

```
transfer_function_dB = meas_power_dBm – power_setting
```

Coarse measurement (all slots, all channels, DDS scale = 0.7, sample rate = 30 MHz, bandwidth = 18 MHz):

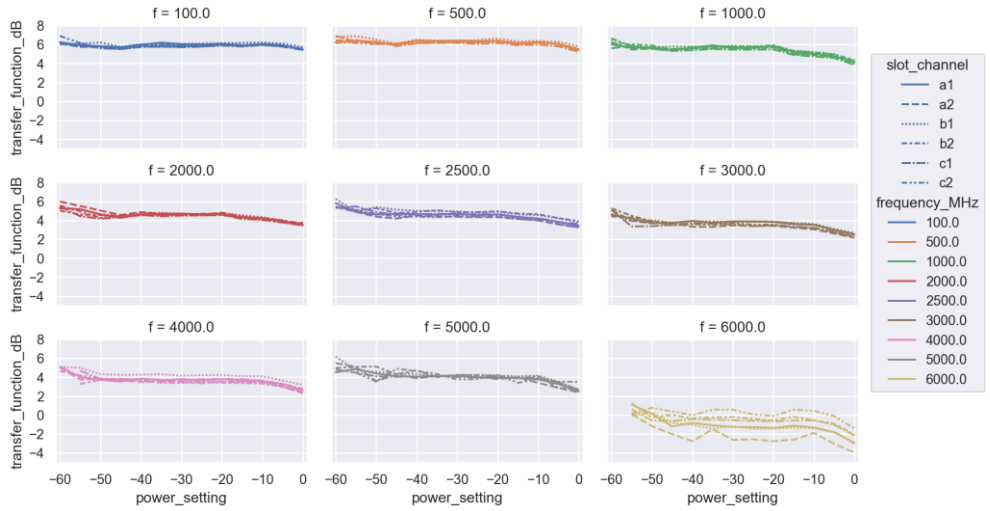

Figure 10.1: Typical TX PWR vs. Power_Setting and Frequency

The output power is approximately 4-6 dB above the power setting at most frequencies. The power control is linear in the range from -55 to -20. Above this, the output starts compressing slightly.

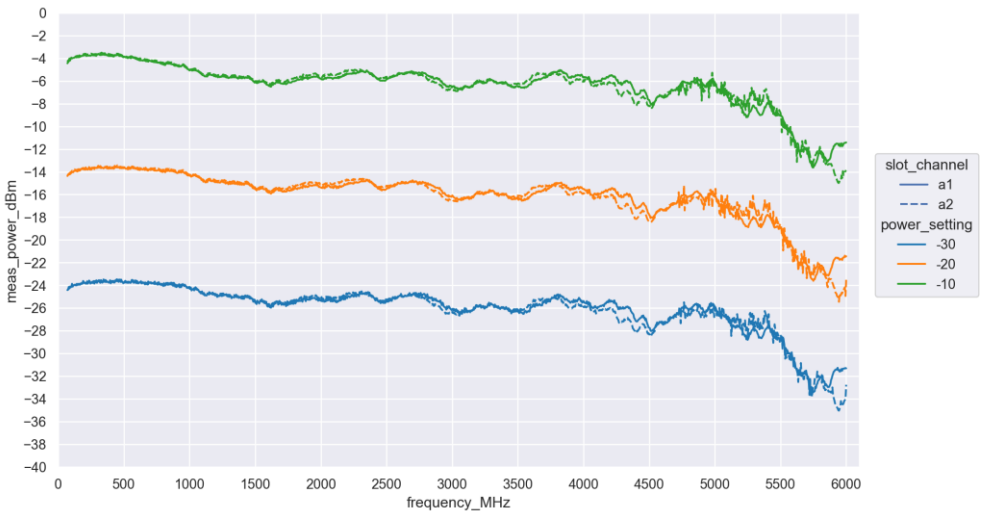

Figure 10.2: TX power vs. frequency and power_setting

The TX power is within +/- 3 dB up to 5500 MHz.

10.4.1.1 TX power vs. temperature

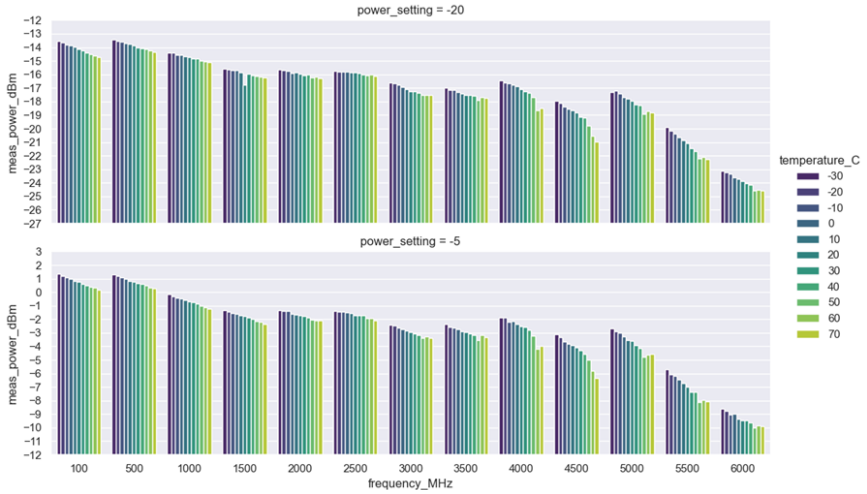

Figure 10.3: TX power vs. temperature

Typical power variation is -1 dB/100°C

10.4.2 TX Harmonics

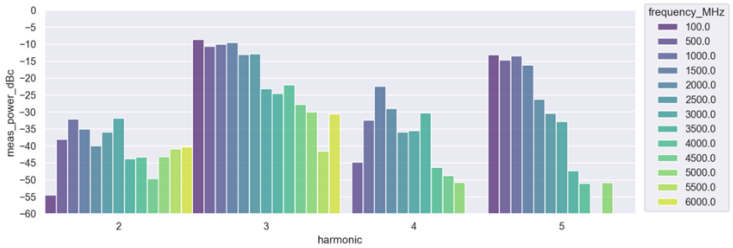

Figure 10.4: TX harmonics expressed as a level relative to the fundamental (dBc)

10.4.3 TX wideband emission

Typical wideband emission (all slots, all channels, scale = 0.7, sample rate = 30 MHz, bandwidth = 18 MHz, colors indicate the min/median/max across slots and channels – the min and max traces have been shifted -0.25 GHz and +0.25 GHz, respectively, so the traces do not mask each other):

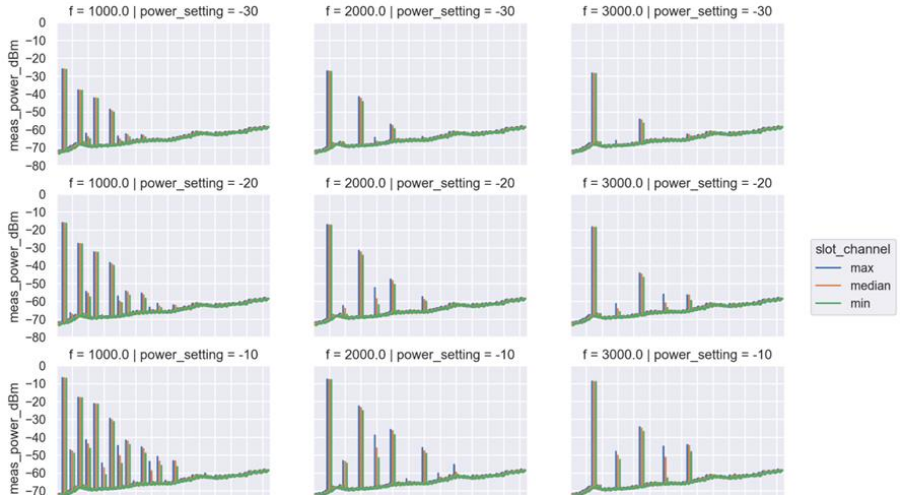

Figure 10.5: TX wideband emission

10.4.4 TX wideband reference clock spurious

Reference clock creates spurious on the TX output. Below a measurement of spectrum in 10 MHz increments to hit all multiple of the 40 MHz reference clock.
Measurement settings (all slots, scale = 0.7, sample rate = 30 MHz, bandwidth = 18 MHz, TX power -10 dB).
The measured frequencies have been divided four groups depending on how far they are from a multiple of 40 MHz – for example {40, 80, 120} MHz are 0 MHz offset from a multiple of 40 MHz while {50, 90, 130} MHz are 10 MHz offset from a multiple of 40 MHz. Note that the fundamental and the harmonics of the fundamental have been removed from the trace to focus on the clock spurs.

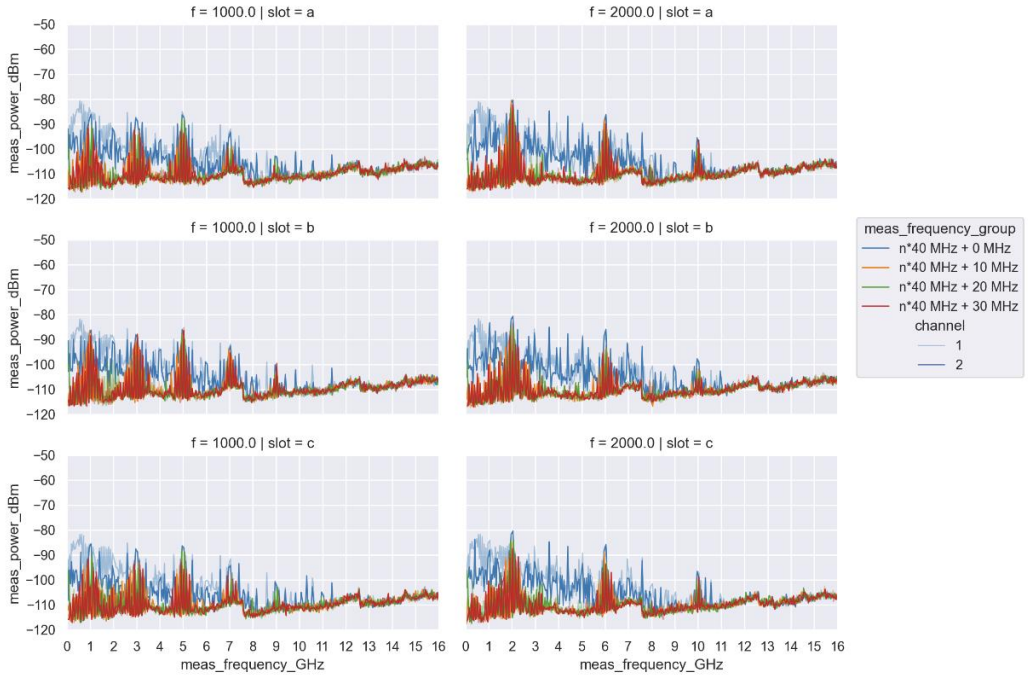

Figure 10.7: TX reference clock spurious level

10.4.5 TX spurious emission – Near carrier

The below figure shows the spectrum with a 1 MHz tone modulated to the carrier.

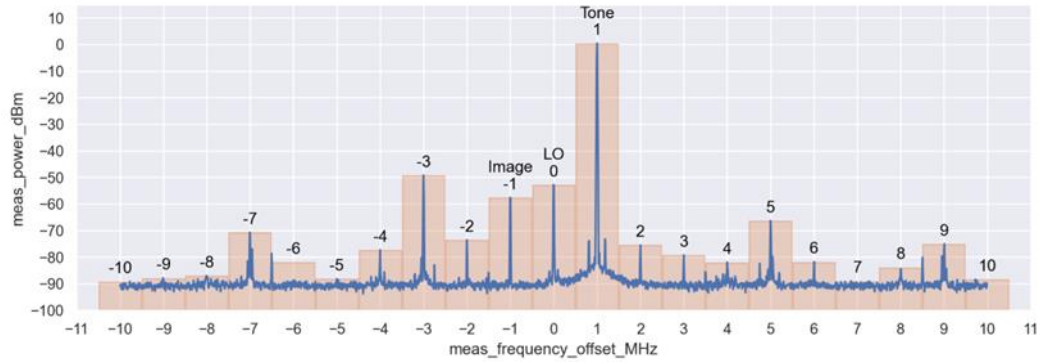

Figure 10.8: TX spurious near carrier. TX scale 0.7

10.4.6 TX Error Vector Magnitude (EVM)

The EVM is generally below -30 dB. Typical values below.

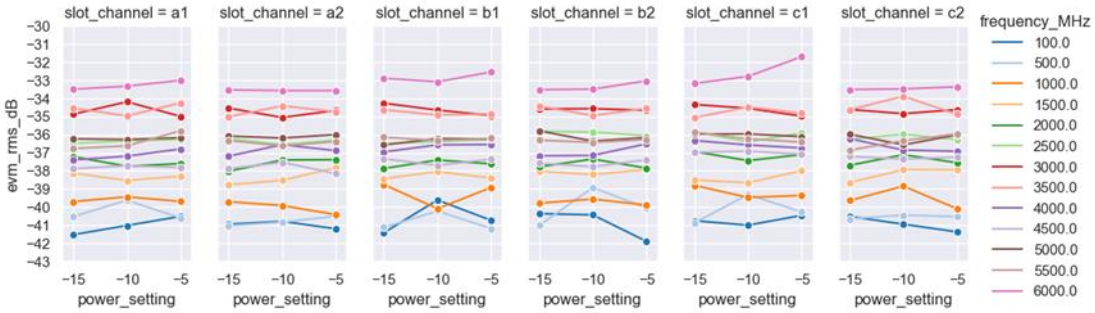

Figure 10.9: Typical EVM values. TX scale_setting 0.7

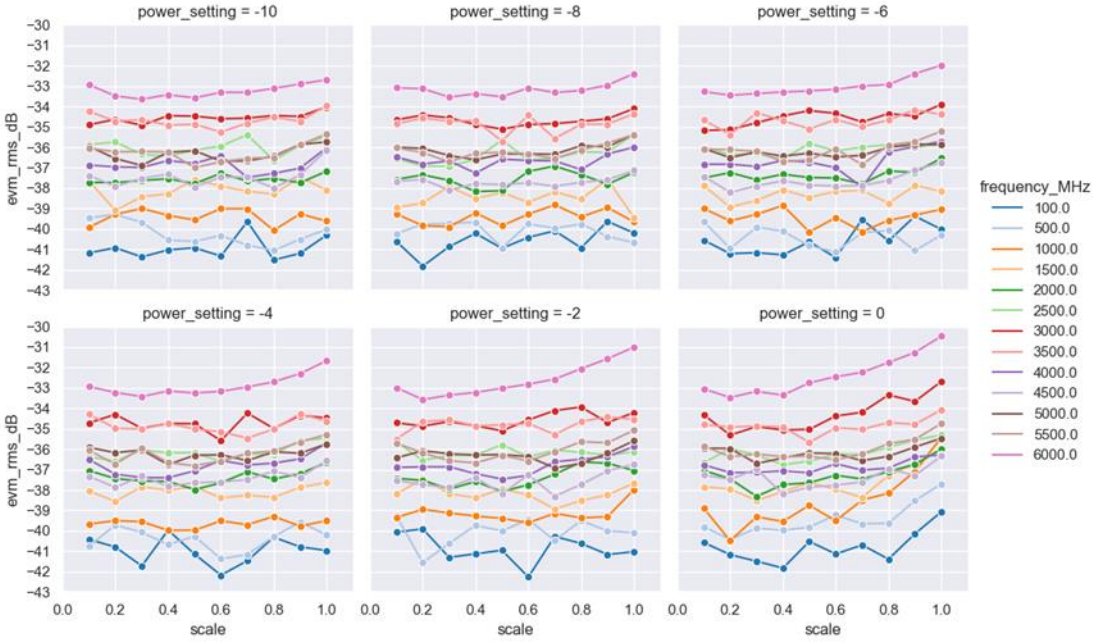

Figure 10.10: Typical EVM vs. power_setting vs. scale_setting

10.4.7 RX Gain

The TR600 modules RX input has various gain settings vs. LO frequency settings.

The RX chain of the TR600 consists of multiple adjustable gain stages in series. The idea behind this configuration is to obtain a linear gain range in 1 dB steps by combining the different gain steps. This is implemented as a “gain table”, which for each index in the table contains the setting for each gain stage. The rows in the table will then step in 1 dB increments (ideally).

RX LO range [MHz]	Minimum gain [dB]	Maximum gain [dB]
70 – 1300	-1	73
1300 – 4000	-3	71
4000 – 6000	-10	62

Table 10.4.5: RX Gain

The gain stages are shown below (from the AD9361 Reference Manual UG-570):

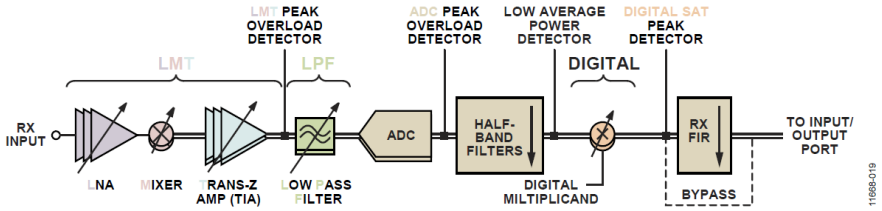

Figure 10.11: TR600 RX Gain stage Block Diagram

The TR600 receiver has a build in RSSI indicator.

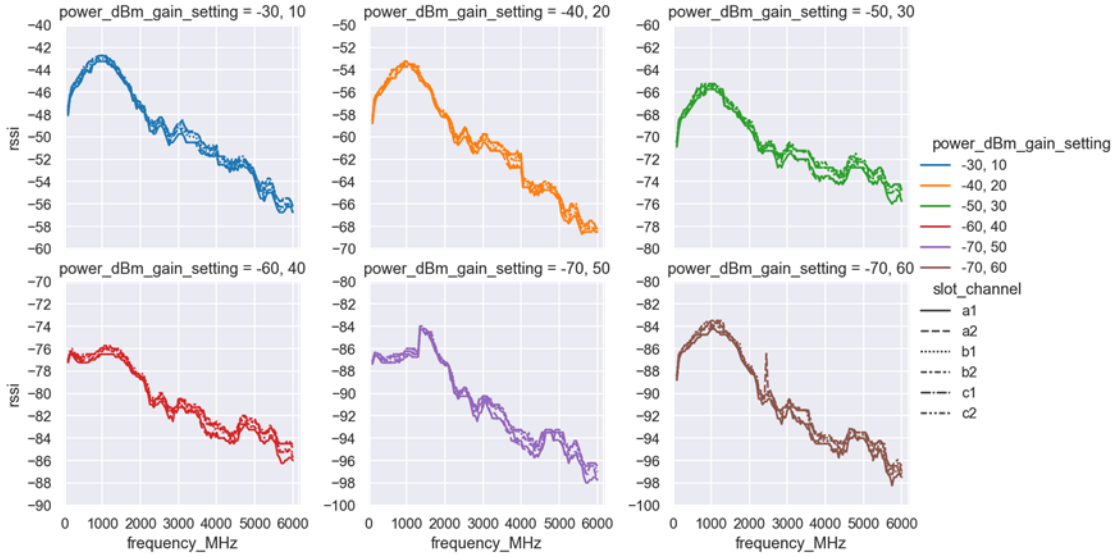

Figure 10.12: Typical RSSI report vs. power input and RX gain settings

The RSSI indicator is calculated based on the digitized I/Q signals.
The TR600 has an Automatic Gain Control (AGC) that dynamically can keep a stable I/Q level.

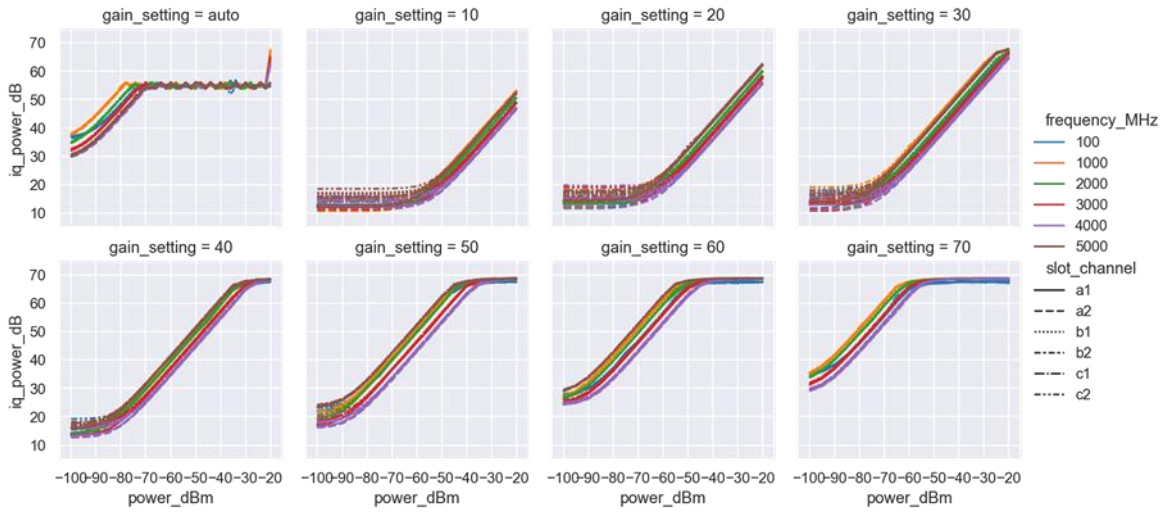

Figure 10.13: I/Q level vs. input power. Auto gain settings vs. fixed gain setting

10.4.8 RX filter response vs. bandwidth.

The TR600 has an internal programmable analog filter for pre-filtering of the received signal before ADC conversion.

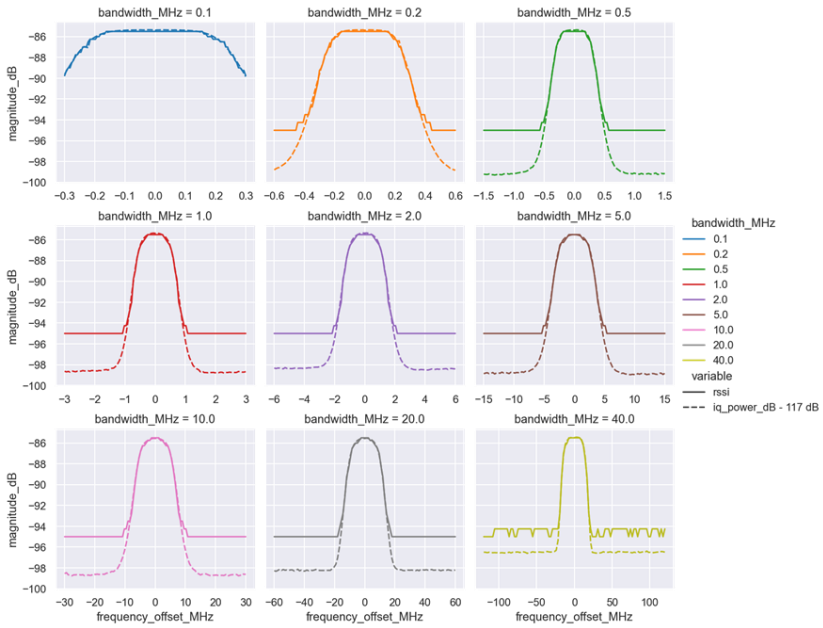

Figure 10.14: RX BW vs. RX filter setting

10.4.9 RX Noise figure.

Noise figure for a receiver like the TR600 stated by using the Y-factor method.
A calibrated noise source is connected to the RX input of the TR-600. The noise source is calibrated so the ENR (excess noise ratio) is known as a function of frequency.

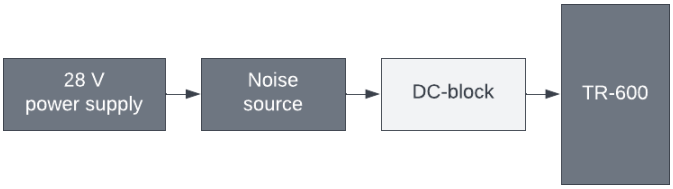

Figure 10.15: RX noise measurement

The RMS “voltage” is measured with the noise source enabled (“hot”) and then with the noise source disabled (“cold”).

As the measurement is done after the ADC, the IQ RMS value is used as a measure of voltage below.

The noise figure in dB is calculated with the following formulas, where *L* is the cable loss between noise source and RX input:

$$\mathrm{ENR} = 10^{\frac{\mathrm{ENR_{dB}}}{10}}$$

$$Y = \left(\frac{V_{\mathrm{rms,hot}}}{V_{\mathrm{rms,cold}}}\right)^2$$

$$\mathrm{NF} = 10\log_{10}\left(\frac{\mathrm{ENR}}{Y-1}\right) - L_{\mathrm{dB}}$$

To avoid any LO leakage in the noise measurement, the IQ samples are first fed through a FIR filter with the following specifications before the RMS value is calculated:

- Type: Complex band pass
- Window type: Hamming
- Number of taps: 31
- Sample rate: 20 MHz
- Pass band: 1 – 4 MHz
- Transition width: 1.5 MHz
- Attenuation at 0 Hz: 40 dB

The noise figure is only presented for gain settings where the gain in the LNA stage (first stage) is above 3 dB as the noise figure otherwise increases to levels where this measurement procedure is inaccurate.

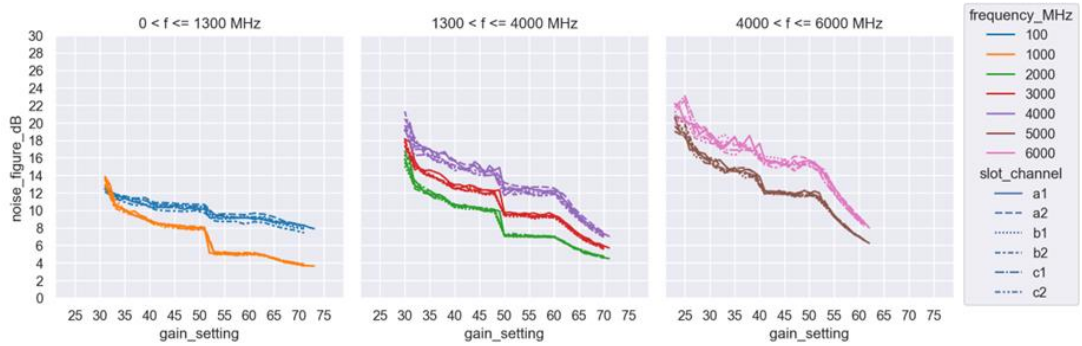

Figure 10.16: NF as function of RX Gain setting

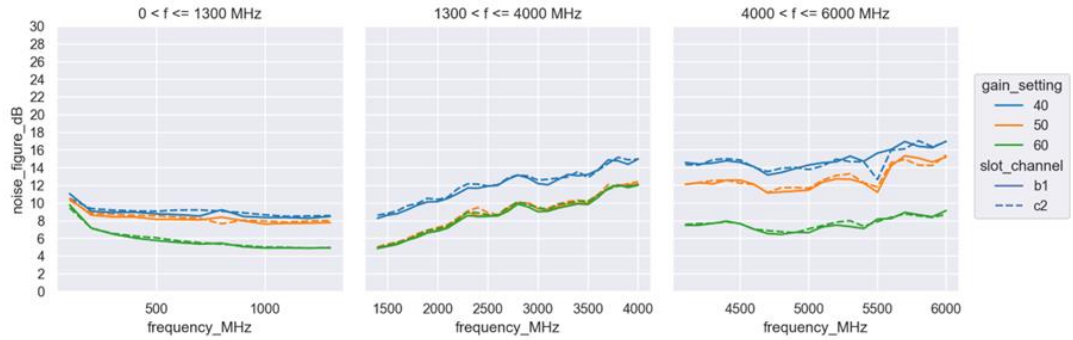

Figure 10.17: NF as function of frequency. Tree fixed gain settings

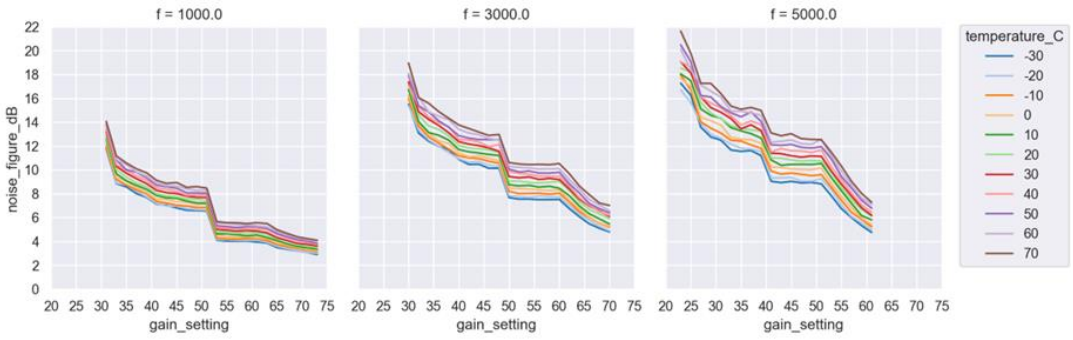

Figure 10.18: NF as function of temperature

10.4.10 RX spurious emission.

RX spurious in this document is stated with the following measurement setup.

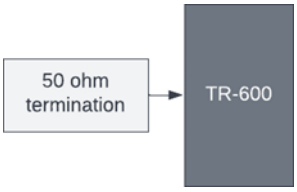

Figure 10.19: RX spurious measurement

Unless otherwise noted, the following settings are used:

- Bandwidth = 50 MHz
- Sample rate = 50 MHz
- Gain setting = maximum for given frequency
- Specified frequencies = Random selected in 1 MHz resolution

The gray traces are the individual slot/channel traces, and the black trace is the maximum across slot/channel. The colored bands mark the frequencies that are multiples of 10 MHz, 20 MHz, and 40 MHz.

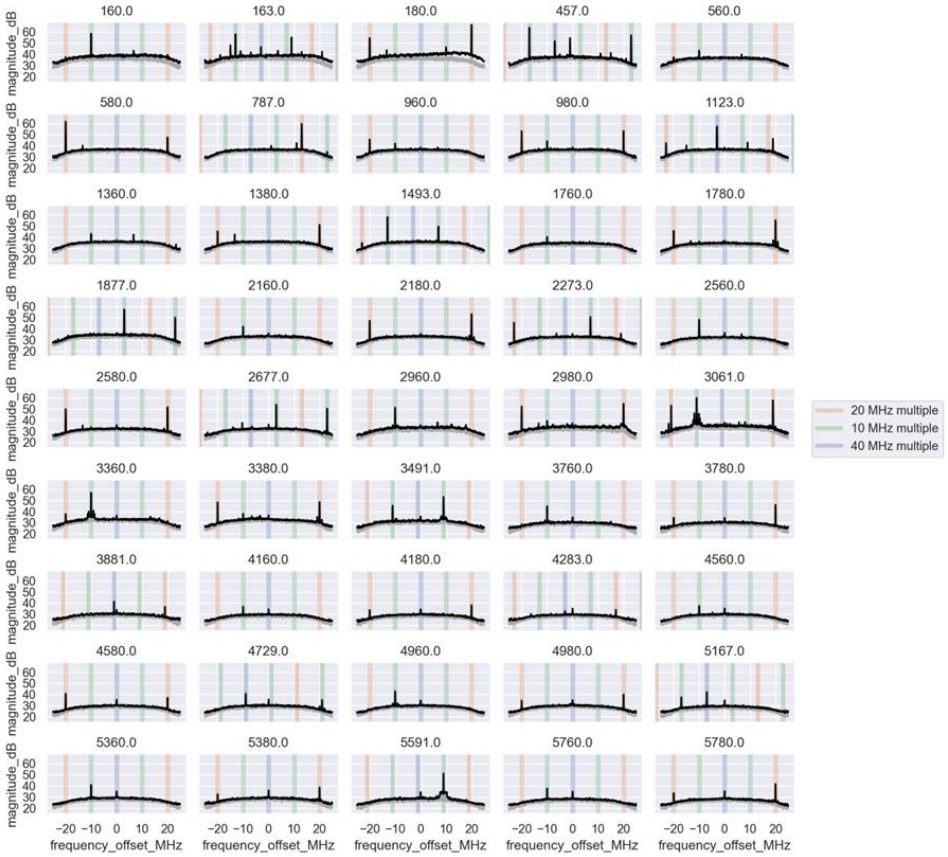

Figure 10.20: RX internal generated spurious

Mostly spurious in the receiver band is multiples of the 40 MHz reference clock and divisions thereof (10 MHz, 20 MHz, 40 MHz).

10.4.11 RX Intermodulation.

Gain setting	300 MHz	400 MHz	500 MHz	1600 MHz	2000 MHz	2500 MHz	3700 MHz	4000 MHz	5000 MHz	6000 MHz
30	-2.6	-3.2	-3.9	-6.7	-4.8	-2.1	-1.5	-1.1	-5.4	-2.2
40	-13.0	-12.9	-12.7	-13.5	-12.0	-10.1	-6.4	-5.4	-13.8	-11.0
50	-23.8	-23.3	-22.4	-24.4	-23.0	-20.5	-17.2	-14.0	-26.4	-21.6

Table 10.4.6: Typical third order intercept point, IIP3 [dBm]

10.4.12 RX input impedance.

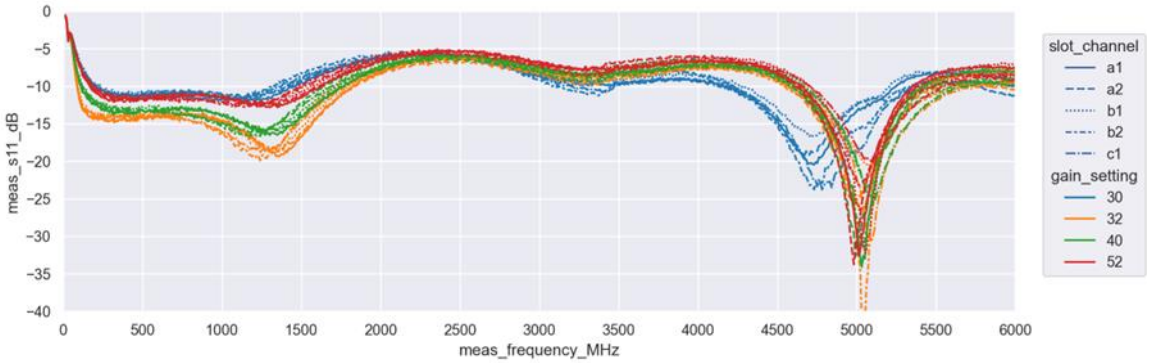

Figure 10.21: Typical S11 [dB]

10.4.13 Distributed clock

TR600 modules are synchronized with the local 40MHz VCTCXO on the NanoCom SDR MK3. It can also be synchronized with an external clock connected on COM-1 or COM-2 (see §9.2 for more details), this can be configured with the development kit.

	Description	Min	Typ	Max	Unit
RX_{FREQ_INIT}	Initial RX frequency error vs temperature	-3.0		+3.0	PPM
RX_{FREQ_AGE}	RX frequency error due to aging	-2.0		+2.0	PPM

Table 10.4.7: VCTCXO frequency stability [ppm]

10.4.14 RX Limitation during boot process

The RX input is supplied with DC current, until the boot process has been finalised. About 20 seconds for Linux boot, then the correct GPOs will be set as default. But during the boot process, the current functionality is that there will be 4.6V DC on the RX input during this time until the SW takes control.

10.5 Multi-Chip Synchronization

Multi-Chip Synchronization, hereafter named MCS, is a HW/SW feature to ensure phase coherence between the receive paths of two or three TR600s in slot A and B or A, B and C.

RF characteristics related to MCS performance are presented as typical measurements in this section. Unless otherwise noted results are from an SDR MK3 equipped with three TR600 in slot A, B and C. T1 TR600 slot B is used to generate the external MCS calibration signal (+2MHz offset) and serve as test generator as well for deriving performance characteristics. T1 TX gain is set to -40 which equals an input level at R1 and R2 slot A, B and C of -45dBm to -55dBm depending on frequency.

Phase deviation characteristics are relative to R1 slot A. Captures of 10000 RX IQ samples at a rate of 61.44Msps, yielding an overall sampling duration of 163µsec, is used to determine phase deviation. RX filter bandwidth is configured to 54MHz and MCS calibration as well as measurements are done with AD9361 RX I/Q quadrature tracking disabled.

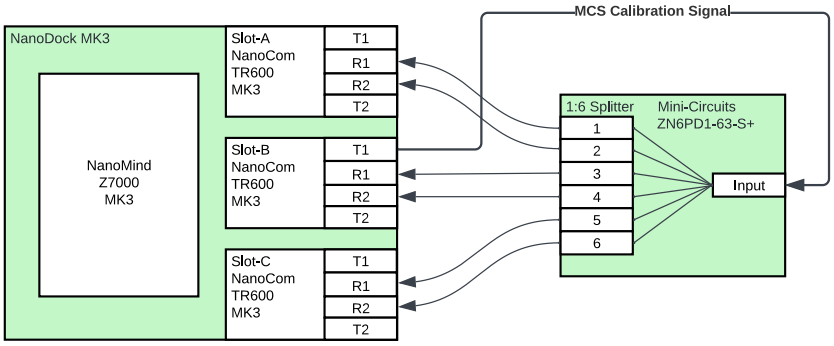

Figure 10.22: MCS calibration and test setup

The amplitude and phase response of the 1:6 splitter including coax harness have been measured from 500Mhz to 3GHz using a Vector Network Analyzer. Amplitude response is within 14dB to 18.5dB, Input to path 1 to 6. Normalized Phase response is within +/-1.5deg for the tested frequency bands in section 10.5.3 RX phase deviation vs frequency. Below is an example for RX frequency 1000MHz +/-25MHz. The black line indicates the MCS calibration frequency. S21 Phase Normalized is relative to path “Input->1” and MCS calibration frequency.

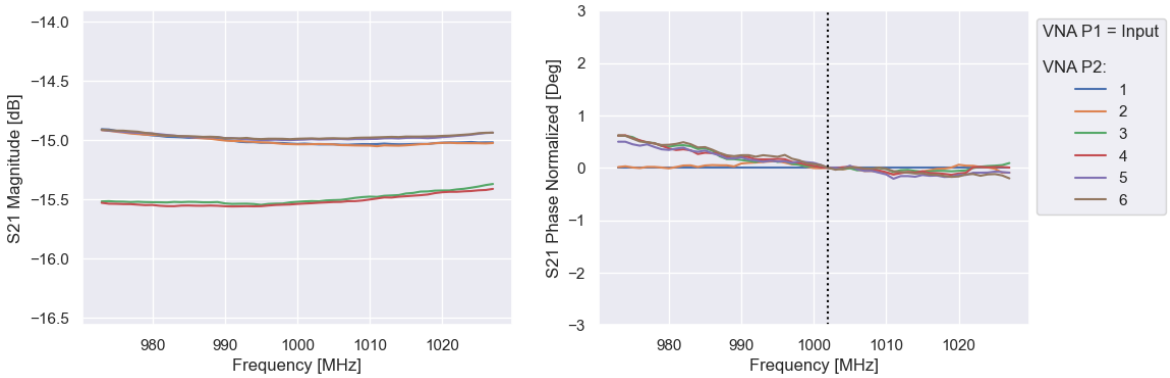

Figure 10.23: Magnitude and normalized phase response at 1000MHz of 1:6 Splitter

10.5.1 High level feature description

The transceiver IC AD9361 utilized in TR600 is equipped with inputs and circuitry to ensure phase coherence across multiple ICs / TR600s at baseband level (ADC sampling).

AD9361 does not include functionality to ensure phase alignment at RF level (of local oscillators used for down conversion) across TR600s or other internal / external delays causing phase skew between individual receive paths. In this case residual phase differences between individual TR600s and RF frontend circuity is determined and corrected based on an external calibration signal.

TR600 in slot B can be used to output a continuous wave based calibration signal. When coupling the calibration signal into the frontend of the receiver at a point common to all receive paths, it is possible to determine and correct up to +/-180deg phase difference between the individual paths at Z7000 FPGA side based on the calibration signal.

Two Python scripts, delivered as part of the PDK included with each SDR, can be used to utilize MCS functionality:

`mcs_config.py`: Ensure phase coherency.

- First step in multi-chip synchronization, implemented in accordance with AD9361 reference manual UG-570.
- Synchronization of AD9361s BBPLL's / RX ADC sampling against a common 40MHz reference clock.
- Calibration of LVDS interfaces carrying IQ samples between TR600s and Z7000 FPGA.

`mcs_calibrate.py`: Ensure in phase alignment.

- External CW calibration signal is output at T1 or T2 TR600 slot B at a frequency which is within the RX bandwidth but offset from the RX LO by 2MHz or more.
- The phase difference between the individual receive paths of the received calibration signal are determined and compensated at FPGA side until they are within +/- 0.1deg average deviation.
- The method allows for phase corrections up to +/-180 deg relative to the phase of the calibration signal.

As a prerequisite all receive paths must be operated in FDD mode and configured identical in terms of RX sample rate, filters, GAIN and RF LO frequency. After that a `mcs_config` followed by a `mcs_calibrate` must be carried out to ensure phase alignment at the frequency of the calibration signal.

10.5.2 RX I/Q time domain

Time domain plots of a RX I/Q sample capture before and after MCS calibration. The capture is at a RX frequency of 1000MHz when receiving a continuous wave tone at +2MHz and +4MHz offsets. Amplitude is normalized to full scale ADC resolution.

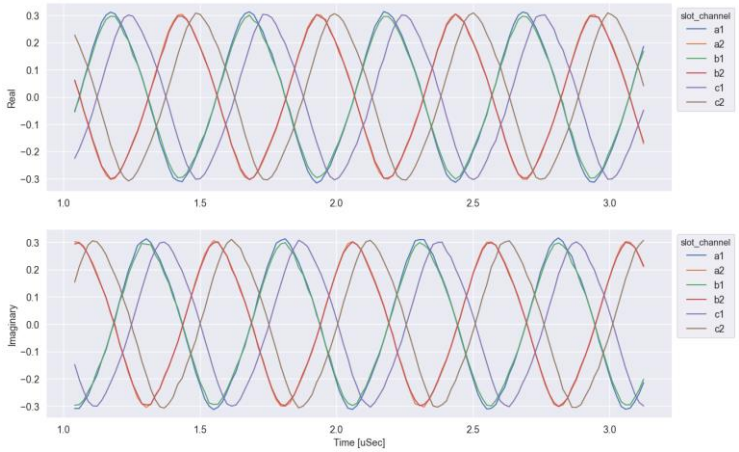

Figure 10.24: RX I/Q samples +2MHz tone after `mcs_config` prior to `mcs_calibration`

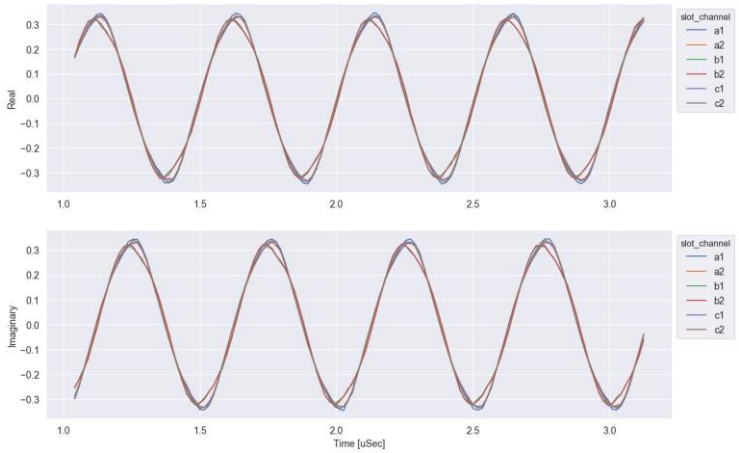

Figure 10.25: RX I/Q samples +2MHz tone after `mcs_calibration`

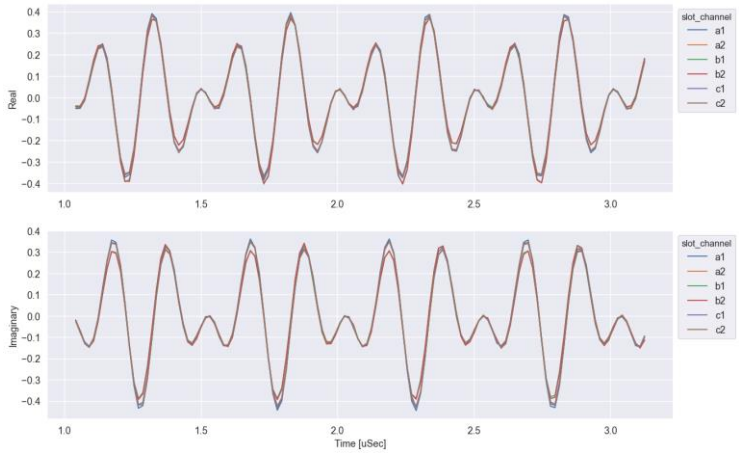

Figure 10.26: RX I/Q samples +2MHz and +4MHz dual tones after `mcs_calibration`

10.5.3 RX phase deviation vs frequency

Phase deviation vs frequency at RX frequency 500, 1000, 2000, and 3000MHz +/-25MHz. Phase deviation is relative to R1 TR600 slot A. Phase deviation vs frequency related to the 1:6 splitter and coax harness are included in the measurement. Typical it accounts for +/-0.5deg phase deviation at the outer frequencies which is considered negligible.

MCS calibration is performed prior to test start at RX frequency +2MHz. The RX gain is fixed at 43. The MCS calibration and test signal is set to gain setting -40 which corresponds to signal level in the range -50dBm +/-5dB at the input of each receive path. The frequency of the continuous wave based test signal is varied +/-25MHz relative to the MCS calibration frequency.

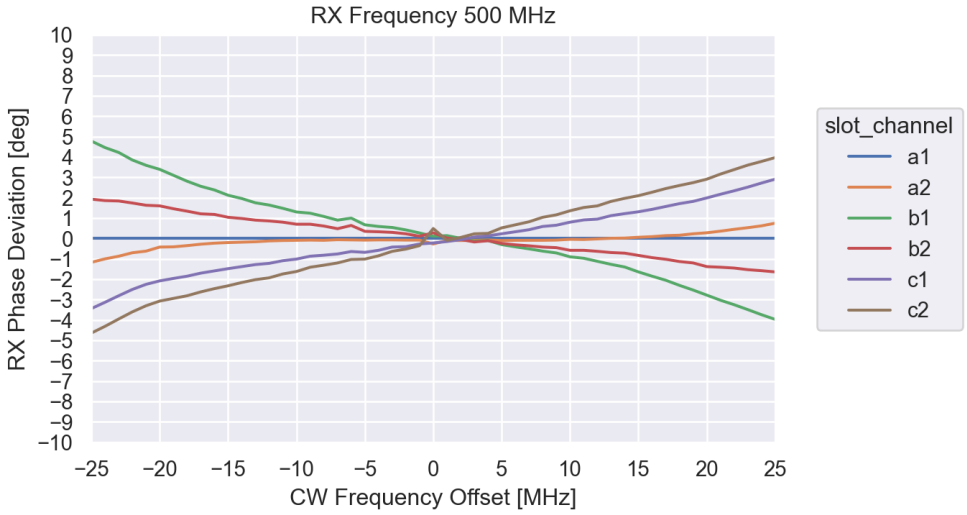

Figure 10.27: RX phase deviation vs frequency at 500MHz

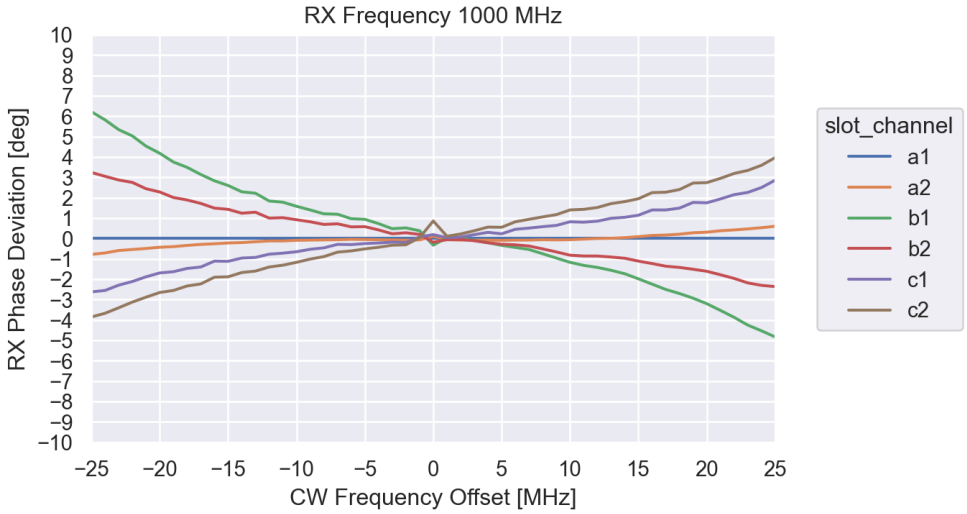

Figure 10.28: RX phase deviation vs frequency at 1000MHz

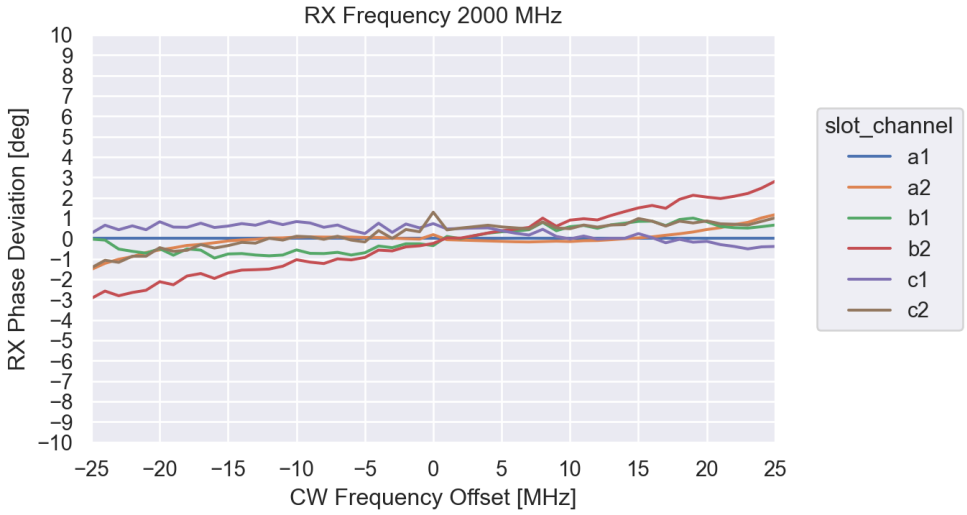

Figure 10.29: RX phase deviation vs frequency at 2000MHz

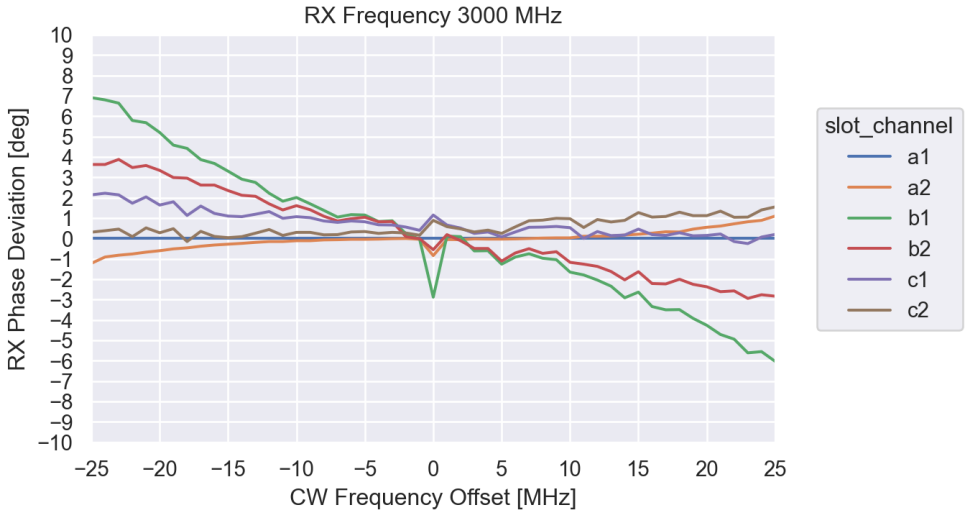

Figure 10.30: RX phase deviation vs frequency at 3000MHz

10.5.4 RX phase deviation vs RX gain

Phase deviation vs gain at RX frequency 500, 1000, 2000, and 3000MHz when receiving a continuous wave tone at +2MHz offset. Phase deviation is relative to R1 TR600 slot A.

MCS calibration is performed prior to test start for each of the tested frequencies at RX gain setting 43. Calibration point is indicated with a dotted marker line below. While keeping the level of the calibration signal constant at gain setting -40, the RX gain is varied manual +/-20dB from the calibration point in steps of 1dB.

The RX chain of the AD9361 consists of multiple adjustable gain stages in series. RX gain settings which cause the LNA input stage in AD9361 to change gain are marked by red dotted lines in the plots below. For further info refer to section 10.4.7. For reference the AD9361 slow attack AGC mode functionality targets an IQ Power of 55dB in FDD mode, see gain_setting = auto plot Figure 10.13

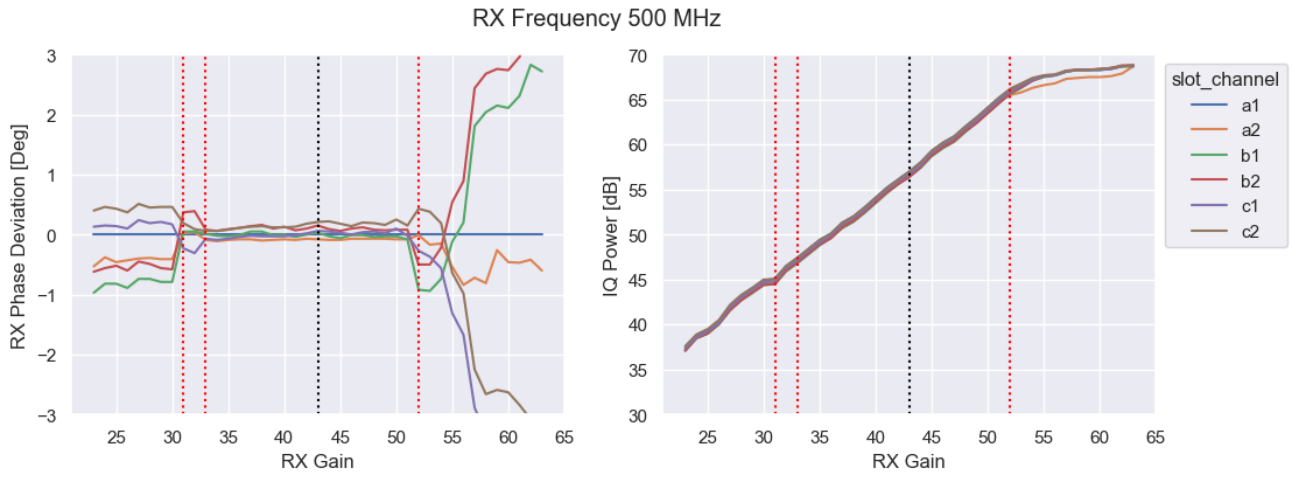

Figure 10.31: RX phase deviation and IQ Power vs gain at 500MHz

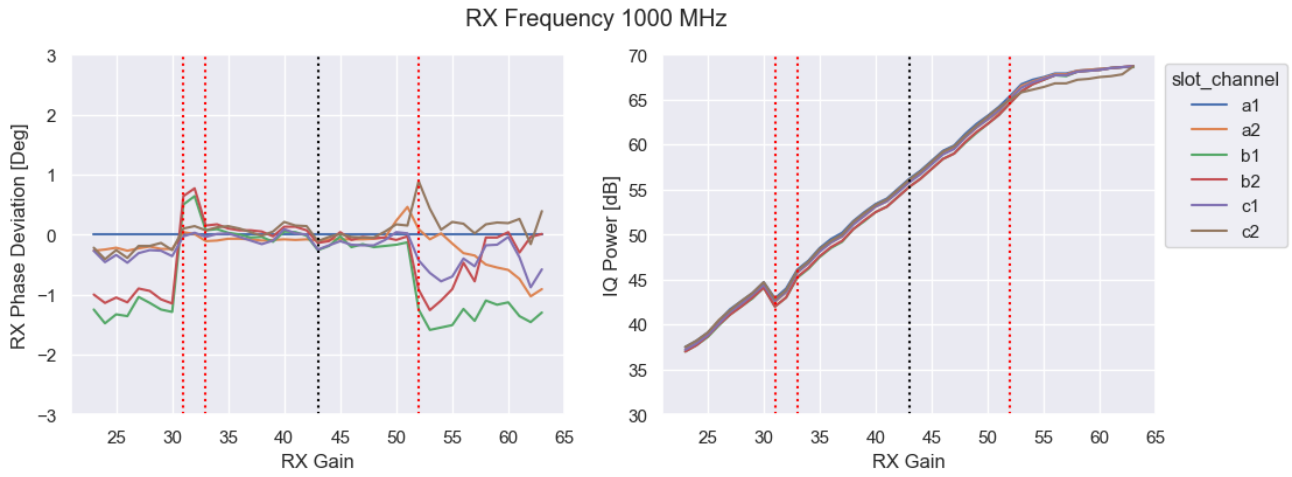

Figure 10.32: RX phase deviation and IQ Power vs gain at 1000MHz

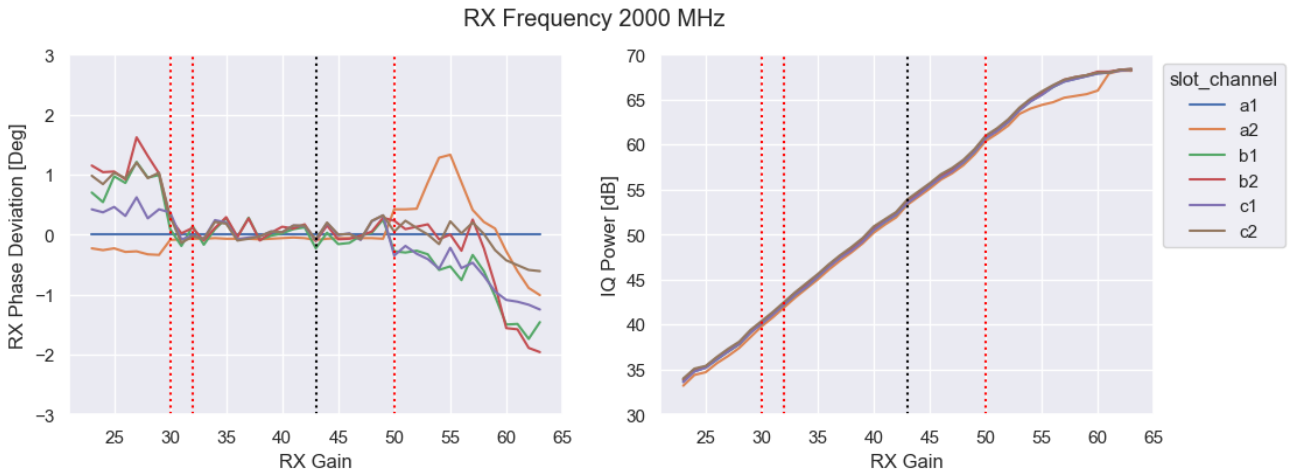

Figure 10.33: RX phase deviation and IQ Power vs gain at 2000MHz

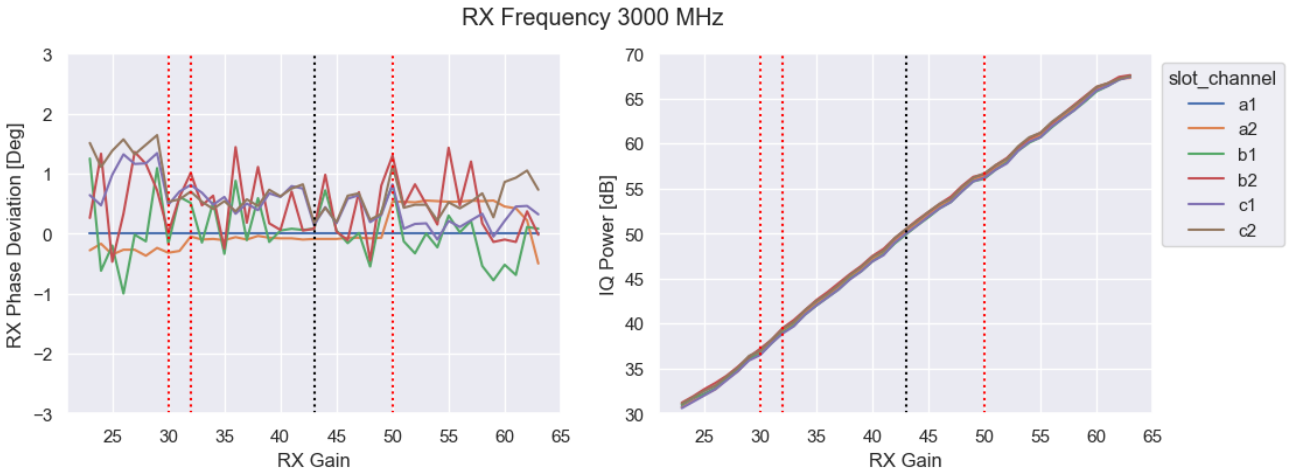

Figure 10.34: RX phase deviation and IQ Power vs gain at 3000MHz

10.5.5 RX phase deviation vs time

Phase deviation vs time at RX frequency 500, 1000, 2000, and 3000MHz when receiving a continuous wave tone at +2MHz offset at constant ambient temperature. Phase deviation is relative to R1 TR600 slot A. Receive path R1 and R2, slot A, B and C are configured for a RX gain of 43. MCS calibration is performed prior to test start for each of the tested frequencies with calibration signal level in the range -50dBm +/-5dB at the input of each receive path.

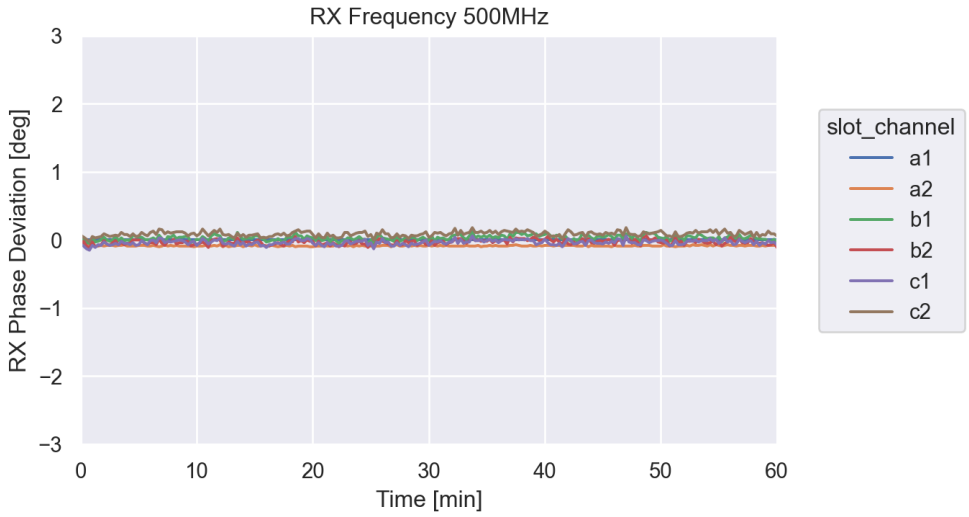

Figure 10.35: RX phase deviation vs time at 500MHz

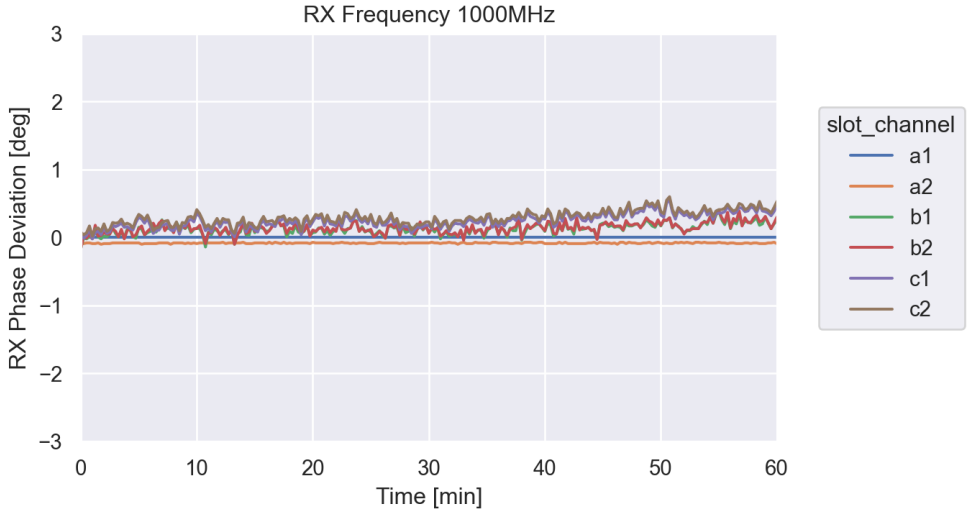

Figure 10.36: RX phase deviation vs time at 1000MHz

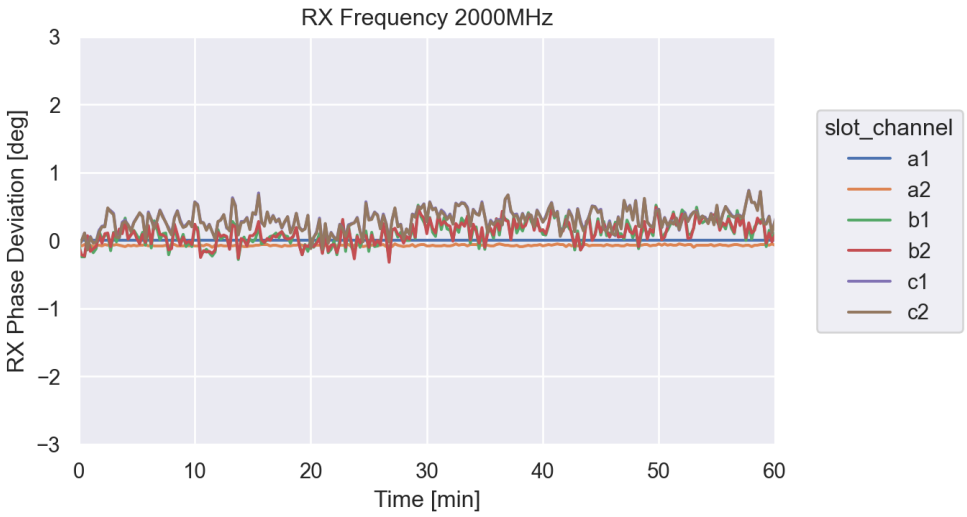

Figure 10.37: RX phase deviation vs time at 2000MHz

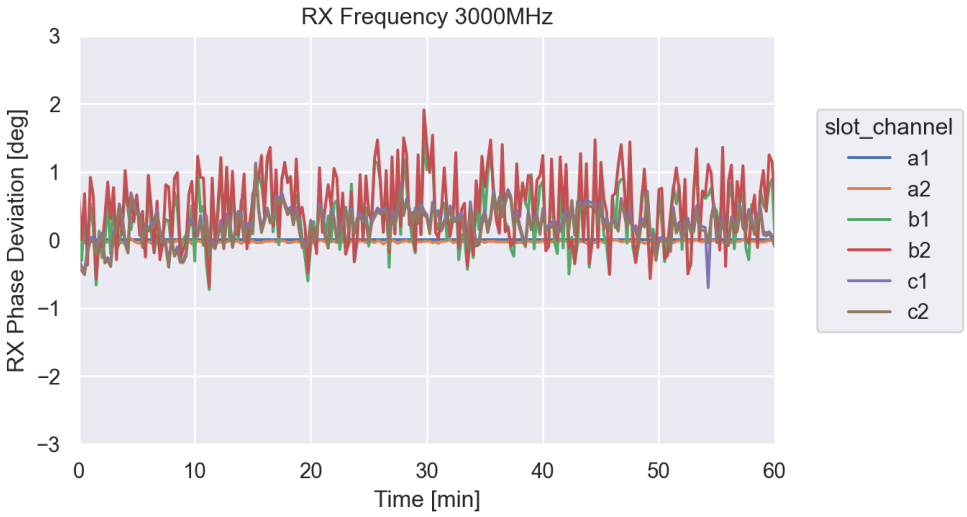

Figure 10.38: RX phase deviation vs time at 3000MHz

10.5.6 RX phase deviation vs temperature

Phase deviation vs temperature at RX frequency 500, 1000, 2000, and 3000MHz when receiving a continuous wave tone at +2MHz offset. Phase deviation is relative to R1 TR600 slot A. Receive path R1 and R2, slot A, B and C are configured for a RX gain of 43.

The MCS setup is placed in a climatic chamber and the ambient temperature is set to -40C. Once stabilised the SDR MK3 is powered and a MCS config and calibration is performed, with calibration signal level in the range -50dBm +/-5dB at the input of each receive path. The climatic chamber in then configured to an ambient temperature of +50C. The sudden change in ambient temperature, together with SDR MK3 self-heating, produces a rapid changing board temperature. Logging of local TR600 temperatures via telemetry indicates a temperature slope of up to +4C/min. Phase deviation is estimated at 15sec intervals for 60min while the SDR exposed to the rapid changing temperature profile.

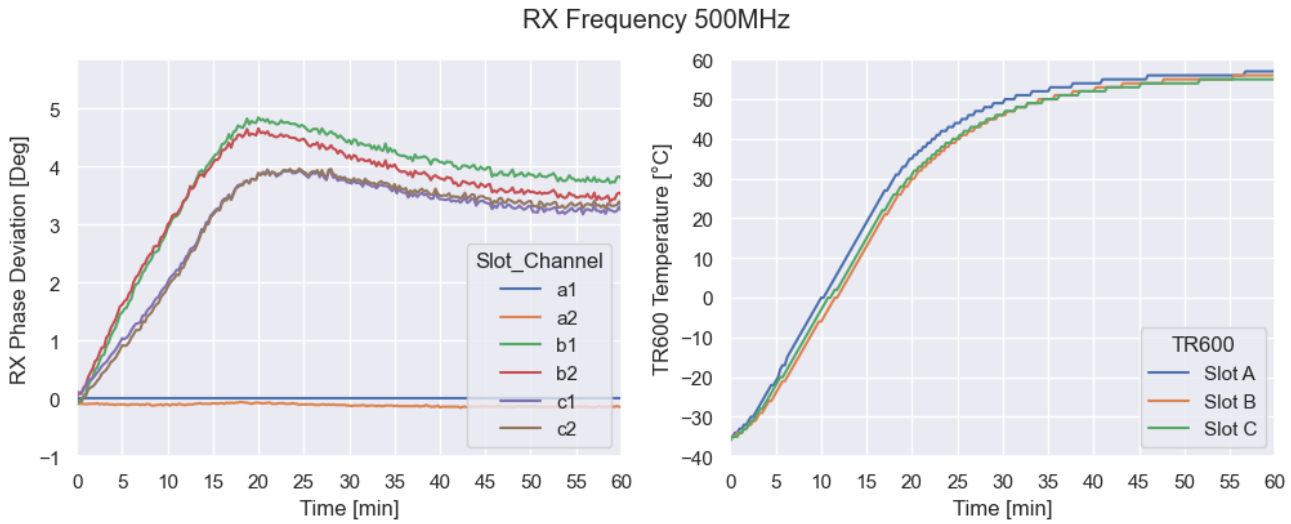

Figure 10.39: RX phase deviation vs temperature at 500MHz

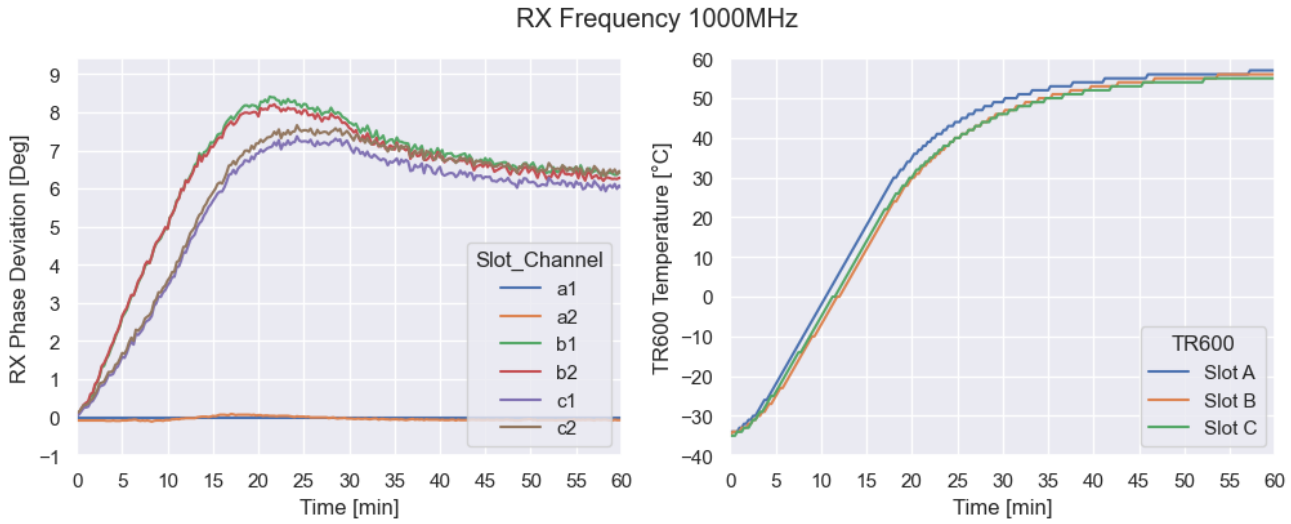

Figure 10.40: RX phase deviation vs temperature at 1000MHz

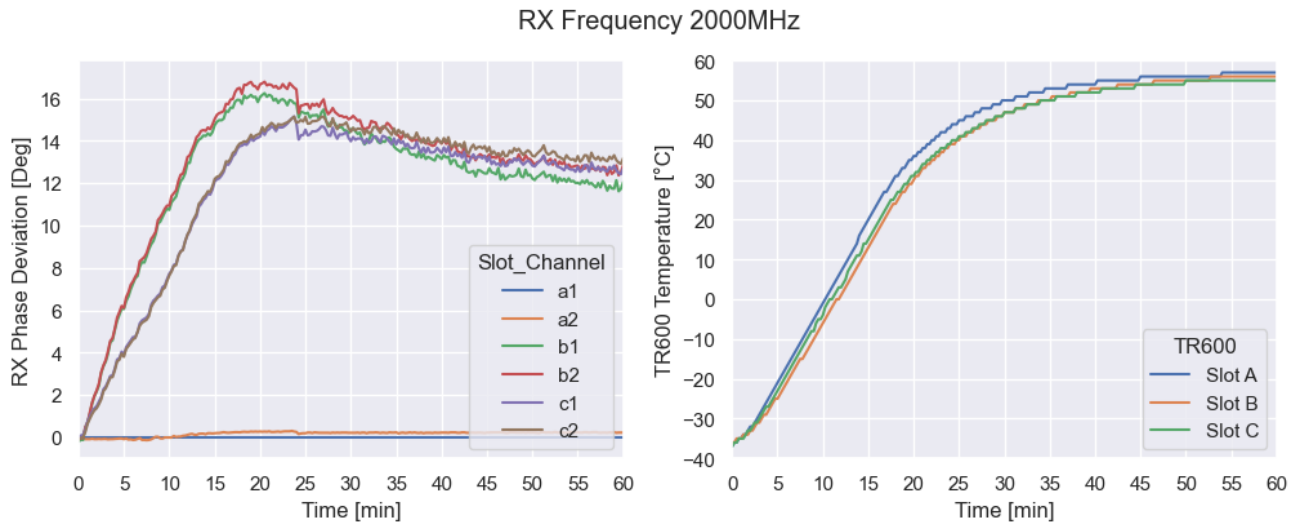

Figure 10.41: RX phase deviation vs temperature at 2000MHz

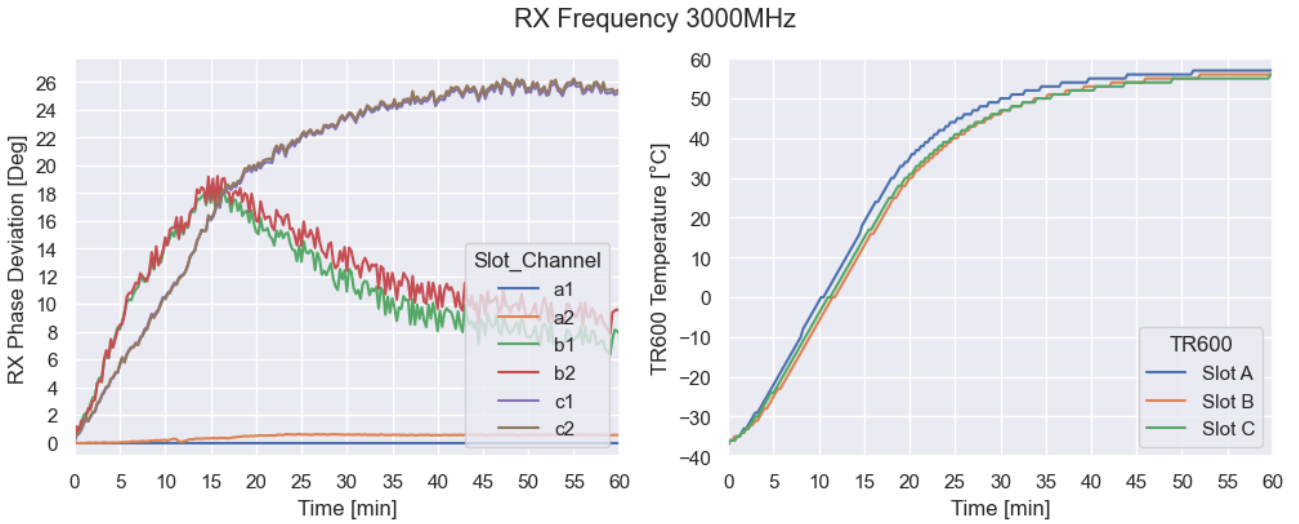

Figure 10.42: RX phase deviation vs temperature at 3000MHz

Phase deviation vs temperature can be compensated by recalibrating MCS. The 1000MHz RX frequency test is repeated below when recalibrating MCS every minute. In this case the highest change in board temperature between consecutive MCS calibrations is +4C, and phase deviation stays within +1/-0.5deg.

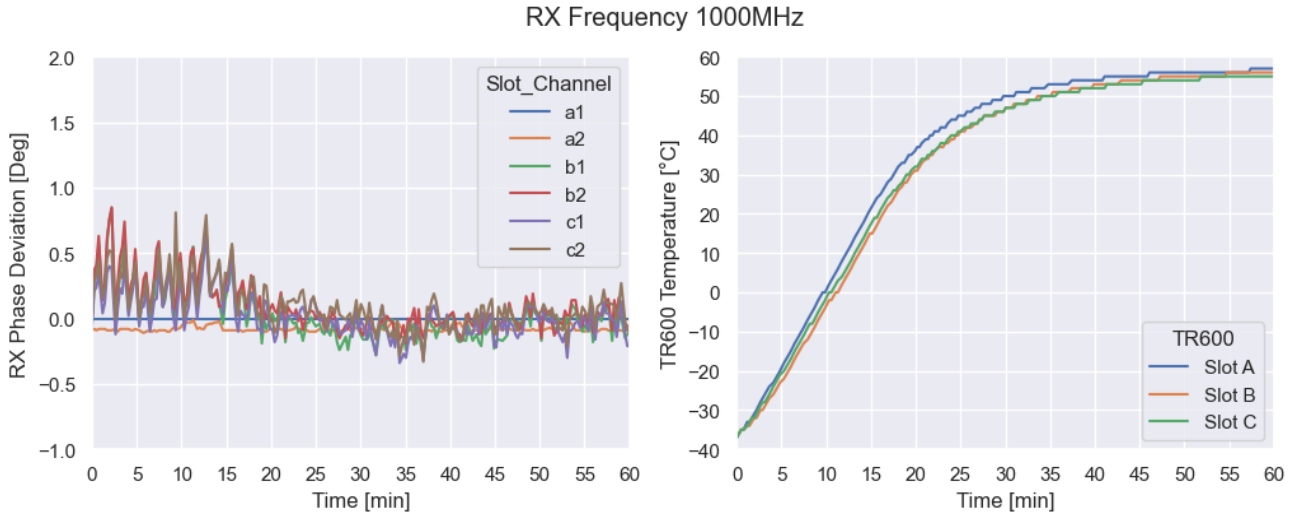

Figure 10.43: RX phase deviation vs temperature at 1000MHz, while recalibrating MCS at 1min intervals

11 Development Kit Overview

The product-design is centered around a Xilinx SoC, overall defined by two “domains”, as defined by Xilinx:

- processing system (PS) – implemented within ARM cores
- programmable logic (PL) – implemented as field-programmable gate array (FPGA) fabric

The radio frequency (RF) aspect of the product is based on a transceiver chip provided by Analog Devices, Inc. (ADI), and the stack supporting this functionality is split across these “domains”. In order to customize- and extend the reference design, GomSpace provides a platform development kit (PDK) as described in the below.

11.1 PDK

GomSpace provides meta information for a complete open-source stack, with U-Boot being the bootloader and Linux the high level operating system (HLOS) and is extended with also transceiver support. The PDK is split in two parts; PL development is facilitated through Xilinx Vivado Design Suite whereas Yocto Project (YP) is the tool used for customizing U-Boot, Linux board support package (BSP), Linux distribution, and associated applications. The relation between these and overall flow is depicted in the Figure 11.1.

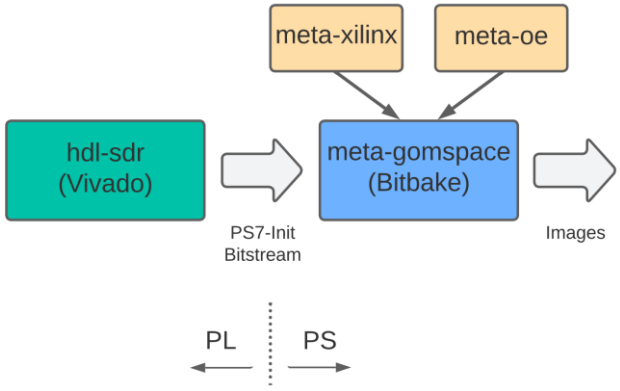

Figure 11.1: Platform Development Kit (PDK)

12 Qualifications

To simulate the harsh conditions of launch and space, the NanoCom SDR MK3 has been exposed to several environmental tests. Contact GomSpace for further information.

13 Disclaimer

The information in this document is subject to change without notice and should not be construed as a commitment by GomSpace. GomSpace assumes no responsibility for any errors that may appear in this document.

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